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Low Temperature Gate Oxidation MOS Transistor Produced by Kr/O_2 Microwave Excited High-Density Plasma

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1. Introduction

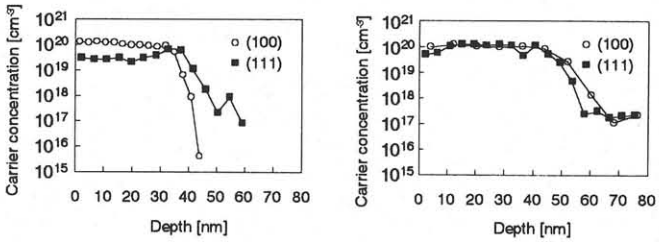
Low temperature processing is a crucial requirement for scaling down of future ULSI (ultra-large-scale integration) semiconductor devices. In this work, it is experimentally demonstrated that MOS transistors produced by low temperature processing of gate oxidation using Kr/O_2 microwave excited high density plasma at 400°C [1] yield comparable I-V characteristics to that of MOS transistors made by conventional dry gate oxidation process grown at 900°C.

2. Experimental

Two groups of MOS transistors, one with dry gate oxidation and second with Kr/O_2 gate oxidation were fabricated under similar processing conditions (except for the gate oxidation step) and silicon substrates. Each group consists of 4 transistor types i.e. (100) P-channel (Ns=1-2×10^{15} cm^{-3}) and (111) P-channel (Ns=1-2×10^{15} cm^{-3}) both phosphorus doped substrates, and (100) N-channel (Ns=3-5×10^{16} cm^{-3}) and (111) N-channel (Ns=1-2×10^{17} cm^{-3}) both boron doped substrates. The gate thickness of all MOS transistors were 10nm. The microwave excited high density plasma oxidation system utilize low ion bombardment energy of less than 7eV and high density plasma above 10^{12} cm^{-3} as well low electron temperature below 1.3eV[4]. The mixing partial pressure ratio of Kr/O_2 was 97/3 and total pressure in the oxidation chamber was 1Torr. The plasma excitation frequency was 2.45GHz. The power density was $5W/cm^2$ as determined by the ratio of the microwave input power and the area of the horn antenna. The silicon substrate temperature during oxidation was 400°C. Additional low temperature step was the post implantation annealing which was preformed at 600°C for 1hour. The implantation was carried out using beam energy and dose of 25keV, 2×10^{15} cm^{-2} respectively, of arsenic (As) on the n-channel and BF_2 on the p-channel transistors. These two low temperature steps are considered to be very important ones towards the achievement of total low temperature processing of MOS devices. This is because they constitute the two most sensitive electronically active parts of the MOS. All other state of the art fabrication steps such as field oxide (1000°C), the LPCVD poly-Si of the gate electrode (550°C) and dopant activation annealing (800°C), the APCVD back contact PSG (for the N-substrate) , BSG (for the P-substrate) were deposited and annealed at 400C° and 1000°C respectively.

3. Results and Discussion

Fig. 1(a) and Fig. 1(b) show carrier profile of the boron and arsenic implanted dopants respectively. Both show shallow junctions with steep dopants profile of about maximum of 60nm resulting from the low post implantation annealing temperature. Fig. 2(a) and Fig. 2(b) show the Id-Vd characteristics of the p-channel (100) and (111)

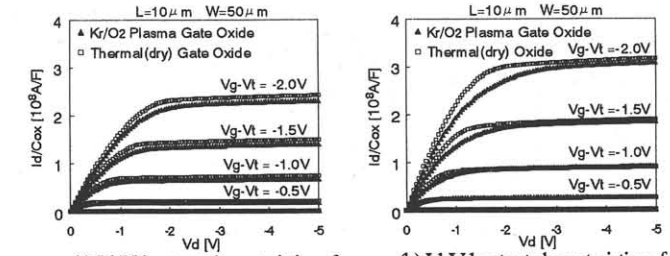


(a) carrier profile of the implanted Boron into (100) and (111) Si substrates

(b) carrier profile of the implanted Arsenic into (100) and (111) Si substrates

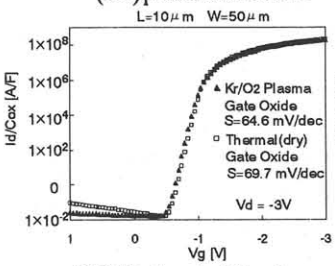
Fig. 1 carrier profile of the boron and arsenic implanted dopant

transistors respectively. Three points are observed, the first being that in each transistor the normalized drain currents (Id/Cox) in the saturation region for the same Vg-Vt exhibit very close values. The second is that the currents in the saturation region (for the same Vg-Vt) in the (111) transistors are higher than that of (100) transistors. This arises from the anisotropy of the field effect mobility of holes in the p-channels[2], i.e. the mobility of holes in the p-channels of (111) and (100) transistors are different. These mobilities have different values than those of the Hall mobilities and those of the bulk conductivity(drift) mobilities[2]. In the transistors of Fig. 2(a) and Fig. 2(b), it is found that the ratio between Id(111)/Cox and Id(100)/Cox

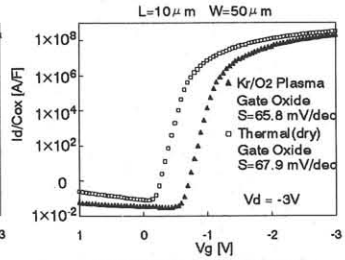


(a) Id-Vd output characteristics of (100) p-channel MOSFET

(b) Id-Vd output characteristics of (111) p-channel MOSFET

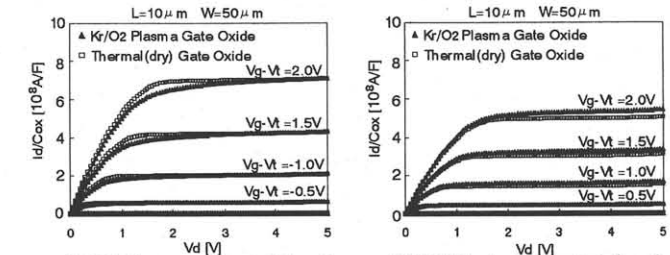


(c) Id-Vg characteristics of (100) p-channel MOSFET



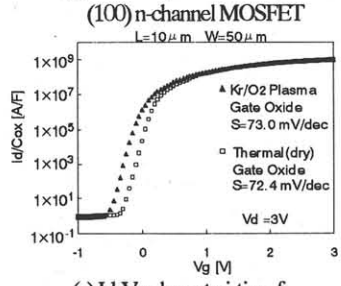
(d) Id-Vg characteristics of (111) p-channel MOSFET

Fig. 2 characteristics of p-channel MOSFET

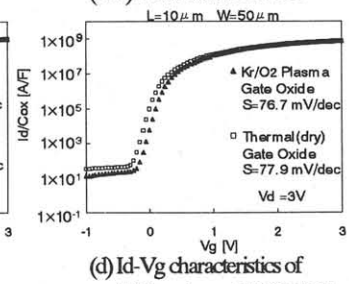


(a) Id-Vd output characteristics of (100) n-channel MOSFET

(b) Id-Vd output characteristics of (111) n-channel MOSFET



(c) Id-Vg characteristics of (100) n-channel MOSFET



(d) Id-Vg characteristics of (111) n-channel MOSFET

Fig. 3 characteristics of n-channel MOSFET

for the same (Vg-Vt) is comparable to $\mu_{pf}(111)/\mu_{pf}(100)$. μ_{pf} indicate the field effect hole mobility within the p-channel. For example in the transistors of Fig. 2(a) and Fig. 2(b), the normalized current ratio of the (111) and (100) transistors in the saturation region for Vg-Vt = -2V is about 1.3 for both the Kr/O_2 and the dry oxidation gates which is close to the ratio of the respective field effect mobilities in their p-channel transistors[2]. The third point is observed in the linear region of the output characteristics i.e. that the internal resistance of the Kr/O_2 transistors is somewhat higher than that of conventional dry oxidation transistor. However in the case of (100) transistor this difference in the internal resistance is smaller and the curves of both transistors are closely matched. Fig. 2(c) and 2(d) show the normalized drain current (Id/Cox) as a function of the gate voltage Vg for the (100) and (111) p-channel MOS respectively. As indicated in Fig. 2(c) and Fig. 2(d) the S-factors of the two Kr/O_2 transistors are quiet similar and the same is true for the two dry oxidation transistors. Also for the (100) case of Fig. 2(c) is can be seen that the curves are closely matched.

Fig. 3(a) and Fig. 3(b) show the output characteristics of the (100) and (111) n-channel MOS transistors respectively. In the (111) case the Kr/O_2 transistor exhibits higher drain current than the that of dry gate oxide transistor demonstrating better current drive ability for the same (Vg-Vt). The (100) transistors (Fig. 3(a)) show higher drain currents in the saturation region than the (111) transistors (Fig. 3(b)) for the same (Vg-Vt). Again this results from the anisotropy in the field effect electron mobility in the respective n-channels[3] which have different values in the (111) and (100) substrates. For example in the transistors of Fig. 3 it was found that the ratio of (Id/Cox) of the (111) transistor to (Id/Cox) in the (100) transistor in the saturation regions, for Vg-Vt=2V is 0.71 for the dry gate oxidation transistor and 0.76 for the Kr/O_2 gate oxidation transistor. These numbers are within the range of the ratio of the respective electron field effect mobilities within their n-channels[3]. Fig. 3(c) and Fig.3(d) show the normalized drain current as a function of Vg for the (100) and (111) transistors respectively. As can be seem the S-factors for (111) n-channel transistors are somewhat higher than those of the (100) n-channel transistors.

4. Conclusions

It is concluded that a reliable thin gate oxide can be produced by the Kr/O_2 microwave excited high density plasma growth techniques which yield MOS characteristics comparable to MOS transistor with a gate which was made by the conventional dry oxidation.

Finally it was shown that the difference in the characteristics of the (111) and the (100) transistors of both gate oxide types results from physical effects rather than technological effects, namely it arises from the difference in their respective carrier channel mobilities and not as a result of processing effects.

References

[1] M. Hirayama, K. Sekine, Y. Saito, and T. Ohmi, Technical Digest, 1999, IEDM, Washington, DC, p249.

[2] T. Sato, Y. Takeishi, and H. Hara, Japan. J. Appl. Phys. 8, p.588 (1969).

[3] T. Sato, Y. Takeishi, and H. Hara, Physical Review B Vol.4, Number 6, p.1950 (1971) .

[4] T. Yamamoto, N. T. Chien, M. Ando, N. Goto, M. Hirayama, and T. Ohmi, Jpn. J. Appl. Phys., Vol.38, pt. 1, No.4A, 1999, p.2082.