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Dual-Thickness Gate Oxidation Technology with Halogen/Xenon Implantation for Embedded DRAMs

Taro Sugizaki, Atsushi Murakoshi*, Yoshio Ozawa*, Toshiro Nakanishi, and Kyoichi Suguro*

Fujitsu Laboratories Ltd., *Toshiba Corporation, 8 Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone: +81-45-770-3208 Fax: +81-45-770-3210 E-mail: sugizaki@flab.fujitsu.co.jp

Introduction

Embedded DRAMs have recently required dual-thickness gate oxide to be grown on the same wafer. A previous study showed that implanting nitrogen into a Si substrate before oxidation can form dual-thickness gate oxide by reducing the oxidation rate at the implanted region [1]. However, the reliability of this gate oxide degrades for nitrogen doses larger than 5×10^{14} cm^{-2} [2]. Argon or fluorine ion implantation into the Si substrate before oxidation can form thicker gate oxide. This method, however, increases the growth rate by 10% [3,4].

In this study, we investigated dual-thickness gate oxide process for embedded DRAM using fluorine (F), iodine (I) and xenon (Xe) implantations. Shallow implanted F, I, and Xe were found to enhance the oxidation rate. Among them, F was found to show the best electrical characteristics. In this paper, we present new results concerned with halogen and Xe enhanced oxidation and propose a new dual thickness gate oxide process, as shown in Fig. 1.

Experiments

P-type (100) Si wafers of 1 Ω · cm were used. F, I, and Xe ions were implanted through sacrificial oxide into the Si substrate at 5 or 10 keV from 1×10^{13} to 1×10^{15} cm^{-2}. Gate oxides were grown in a furnace by pyrogenic oxidation at 750℃ after the sacrificial oxide was removed. Some samples were annealed in an NO ambient for oxynitridation. Immediately after growing the gate oxides, oxide thickness and damage were evaluated using ellipsometry and THERMA-WAVE, respectively. Depth profiles of implanted ions in Si substrate were measured by SIMS analysis. In order to evaluate the electrical properties, poly-metal gate MOS capacitors and MOSFETs were fabricated. The flat band voltage shift, constant voltage stress TDDB, V_g-I_d, contact resistance, and junction leakage current were measured.

Results and Discussion

Figure 2 shows the implant dose dependence of SiO_2 thickness. Oxide thickness increases abruptly from 1×10^{14} cm^{-2}. The increase in oxide thickness was found to be 20%, 80%, and 50% at a 5×10^{14} cm^{-2} dose for F, I, and Xe implantations, respectively. I implantation is most effective in increasing oxide thickness.

Figure 3 shows THERMA-WAVE signal intensity before and after oxidation for F, I, and Xe implanted Si. Before oxidation, F causes less damages than I and Xe. I causes the same damage as Xe, since the atomic mass is about the same. However, I has larger oxidation rate than Xe. These results suggest that enhanced oxidation of I implanted Si is caused by the effect of halogen in addition to implant damage.

Residual damage after oxidation for F implanted Si is less than that for I and Xe implanted Si.

Figure 4 shows SIMS depth profiles at as-implant (Fig. 4(a)) and after oxidation (Fig. 4(b)). I and Xe atoms remain in the Si after oxidation. However, few F atoms were detected in the Si after oxidation. Furthermore, more than 99% of implanted F atoms were found to outdiffuse to an ambient.

We propose the F diffusion model as shown in Fig. 5. The F atom binding to Si at the interface attracts electrons, weakening the binding energy of Si backbonds. As a result, oxidation is enhanced and F atoms, probably in the form of HF [5], outdiffuse to an ambient through SiO_2.

Figure 6 shows TDDB characteristics under a constant voltage stress. The oxide thickness was controlled to about 5 nm. I and Xe implantations degrade T_{bd} with increasing implant dosage. Conversely, F implantation at 5×10^{14} cm^{-2} or below improves T_{bd}. F implantation at 5×10^{14} cm^{-2} was found to have the highest T_{bd}. In F implantation at 1×10^{15} cm^{-2}, excess F atoms are considered to degrade oxide reliability.

From above results, F implantation was focused on MOSFET characteristics.

In order to evaluate boron penetration in gate oxide, C-V measurements were carried out using PMOS capacitors as shown in Fig. 7. The flat-band voltage value of an F implant at 5×10^{14} cm^{-2} is equal to that of the control oxide. This result indicates no enhancement for boron penetration using the appropriate doses of F.

Figure 8 shows V_g-I_d characteristics for NMOS-FET. The V_g-I_d characteristics for F implantation are equal to that of the control oxide. Figure 9 shows the Kelvin contact resistance characteristics of n^+ contact. The contact resistance for F implantation is lower than that of the control oxide. Figure 10 shows the reverse current-voltage characteristics of n^+/p junctions. F implantation reduces the junction leakage current by one order of magnitude. This result suggests that F ions deactivate silicon lattice defects which result in generation centers.

Conclusions

We have evaluated enhanced oxidation effects by F, I, and Xe implantations. Among them I implantation doubles the oxidation rate of Si. F implantation achieves an increase in the oxidation rate of Si by more than 20%. Moreover, F implantation shows highly reliable dielectric characteristics, low contact resistance, and a low junction leakage current. Consequently, the F implantation process provides us reliable dual-thickness gate oxide that is applicable to embedded DRAMs.

References

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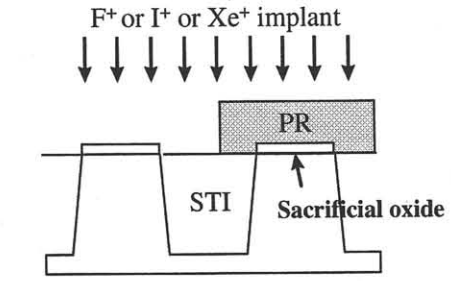
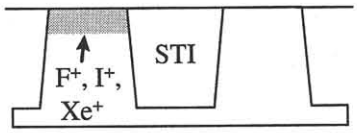
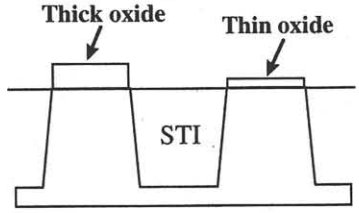


(a) PR patterning and F^+, I^+, Xe^+ implant



(b) Strip PR and sacrificial oxide



(c) Wet gate oxidation

Fig. 1 Process flow for forming dual-thickness gate oxide (PR : Photo Resist)

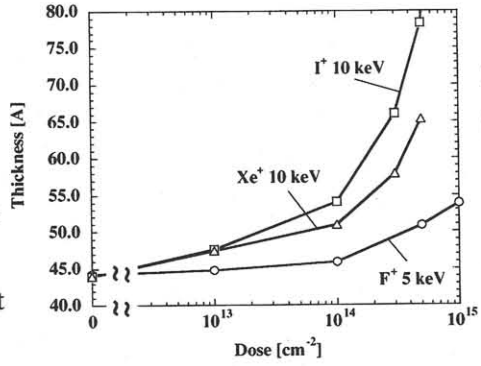


Fig. 2 Thickness dependence on implant dosage

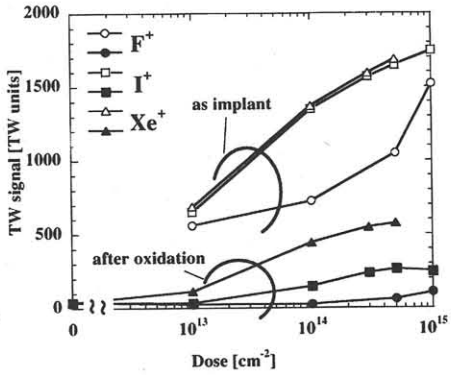
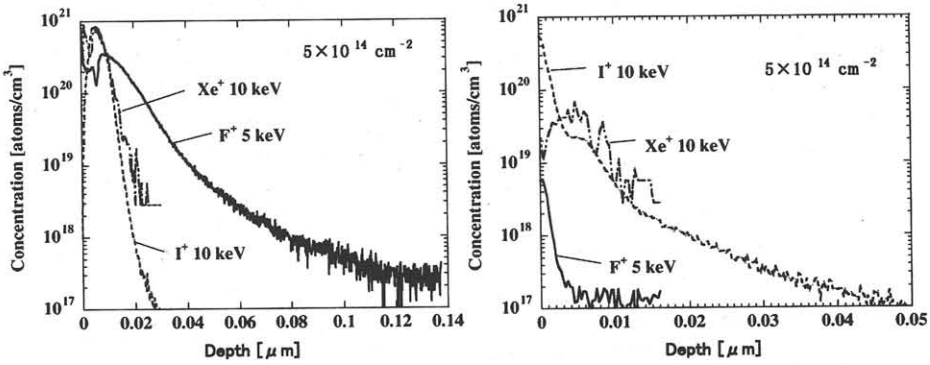


Fig. 3 Damage dependence on implant dosage at as-implant and after oxidation



(a) as implant (b) after oxidation

Fig. 4 Depth profile by using SIMS

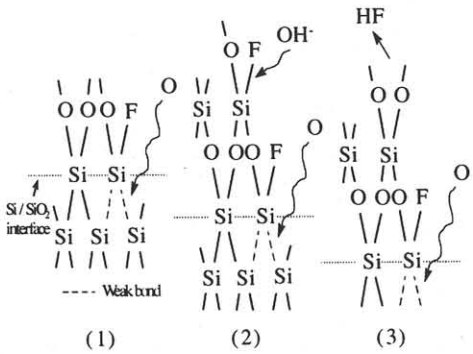


Fig. 5 Schematic diagram of fluorine atom elimination

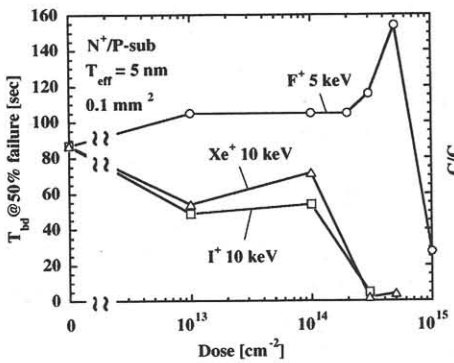


Fig. 6 TDDB characteristics dependence on implant dosage under constant voltage stress at 10 MV/cm

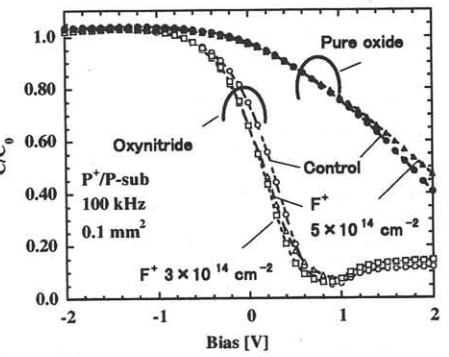


Fig. 7 C-V characteristics of PMOS-diode with boron-doped poly-Si electrode

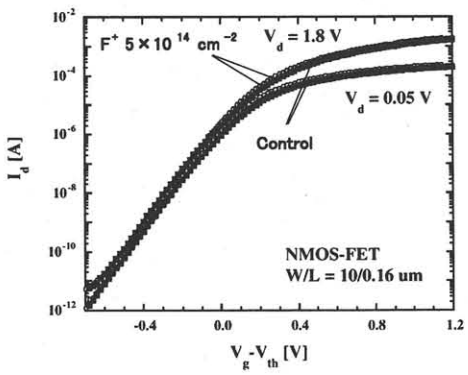


Fig. 8 Vg-Id characteristics of NMOS-FET with F implantation of 5×10^{14} cm^{-2}

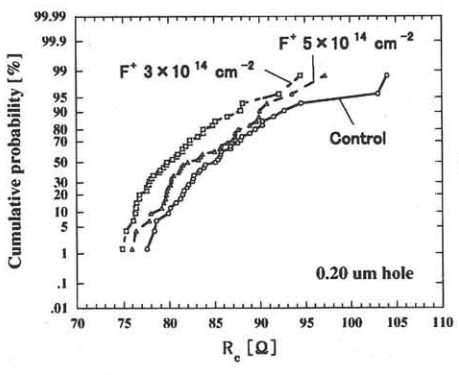


Fig. 9 Cumulative probability of n^+ contact resistance for F implantation

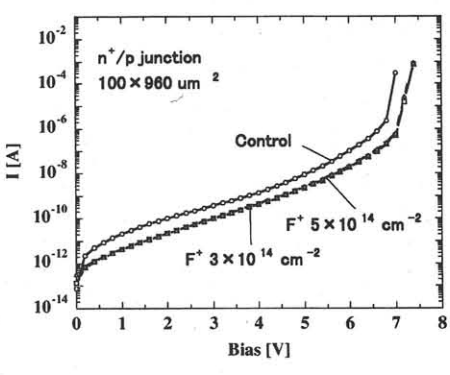


Fig. 10 Reverse current-voltage characteristics of n+/p junctions for F implantaion