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Impacts of Chlorine in CVD-TiN Gate Electrode on the Gate Oxide Reliability in Multiple-Thickness Oxide Technology

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1. Introduction

The metal gate is believed to improve the performance of sub-0.1 μm MOSFETs due to its no gate depletion and low resistivity [1-6]. Refractory metal gate electrodes such as TiN and W are promising candidates because of thermal stability during the subsequent high temperature activation anneal. For the metal gate deposition process, reliability of the gate oxide is a key issue. For the sputtering deposition, formation of the damaged layer at the gate dielectric surface must be suppressed [7-8]. On the other, influence of the impurities in the CVD metal gate on the oxide reliability has to be concerned. Degradation of the gate oxide reliability due to F in CVD-W film for CVD-W/TiN gate MOS capacitor has been previously reported [9].

In this paper, the effects of the chlorine(Cl) residue in the CVD-TiN metal gate on the gate oxide reliability after high temperature anneal are investigated. The Cl diffusion from the TiN into the gate oxide was found to degrade the reliability of the thick oxide, rather than that of the thin oxide, in the multiple-thickness gate oxide technology.

2. Fabrication

The process flow of the TiN gate MOS capacitors is shown in Fig.1. SiON gate dielectric was grown on n-type Si substrate by rapid thermal process at 1050°C using N_2O. The thickness of the oxides were measured to be 2.4 (thin oxide) and 5.6nm(thick oxide) by the spectroscopic ellipsometry, respectively. The TiN gate electrode was deposited by CVD using $TiCl_4$ and NH_3 gas mixture at 650 or 500°C (CVD-1 and CVD-2, respectively). Sputtered TiN gate MOS capacitors was also fabricated (PVD). Anneals at 800, 900 and 1000°C were performed after gate patterning.

3. Results and Discussion

The gate leakage current density (J_g) of CVD-1 with 2.4 and 5.6 nm oxides were evaluated for various annealing temperature (Fig.2). In case of the thin oxide, the J_g slightly decreases as increasing annealing temperature. The J_g of the thick oxide is, however, found to increase after 1000°C anneal. Although the thick oxides with 800 and 900°C anneal have smaller J_g with tight distribution, the J_g for the thick oxide after 1000°C anneal shows a strong increase and a wide distribution (Fig.3). In addition to the capacitors with the typical F-N characteristics (type-B), the capacitors with larger J_g at lower V_{ox} (type-A) were observed(Fig.4). As shown in Fig.5, the numbers of capacitors with the large J_g dependend on gate area. This indicates that the J_g increase is attributed to weak-spot in the thick oxide. The density of the weak-spot which induces the J_g increase is estimated to be about as much as $5x10^5cm^{-2}$. Note that the weak-spot-induced J_g increase is not observable for thin oxide case, due to the large gate tunneling current. In the following, we investigate the J_g increase in the thick oxide in detail.

Two origins can be considered for the observed J_g increase after the high temperature anneal ; (1)the oxide thinning through the reaction between Ti in TiN gate and SiON, and (2)the trap sites formed by the diffusion of *the residual Cl* into gate oxide, originating from $TiCl_4$ during the TiN formation. In order to clarify these points, the thick oxide MOS capacitors with three kinds of TiN gate, i.e., CVD-1, CVD-2 and PVD, were evaluated. The J_g distribution at V_{ox}=3.5V is shown in Fig.6. The PVD samples include no type-A capacitor. On the other, percentage of the type-A capacitor increases for the CVD-2 case. The x values and the residual Cl concentration in the TiN_x gate measured by XPS analysis is shown in Table I. The x values are almost the same for all samples. In addition, no anomalous reaction was observed at the TiN/SiON interface(Fig.7). These results indicate that the weak-spots could not be formed by the silicide reaction between Ti and SiON. The density of the weak-spot had clear correlation with the Cl concentration in TiN gate as shown in Fig.8. Thus, the residual Cl is considered to form weak-spots in the gate oxide after 1000°C anneal, resulting in the J_g increase.

Effects of the residual Cl on the oxide reliability was investigated by constant voltage stress(CVS) TDDB. Figure 9 shows CVS-t_{bd} of CVD-1. For the capacitors annealed at 1000°C, a large number of extrinsic failure is observed. The fraction of extrinsic failure in Fig.9 corresponds to that of the type-A in J_g-V_{ox} characteristics in Fig.4. The t_{bd} of the type-B of 1000°C, on the other, distributes widely, compared to 800 and 900°C annealed samples. Figure 10 shows the time evolution of I_g of the type-B(1000°C), together with that of the 800°C annealed samples. Large increase in I_g and the wider intrinsic t_{bd} distribution of the type-B indicates that the residual Cl which forms the weak-spot, strongly affects the oxide reliability of the type-B. This residual Cl effect is well confirmed from Fig.11. (Stress time dependence of I_g for the type-A.) Current fluctuations during the stress [10] is due to the electron conduction through the Cl-related trap site.

4. Conclusions

Gate oxide reliability of the CVD-TiN metal gate MOS capacitor was investigated. Reliability of the thick gate oxide drastically degraded after 1000°C anneal as compared to that of the thin oxide, which is considered to be due to the trap site formed by the diffusion of Cl residue in the TiN electrode. Controlling of impurities in the CVD metal gate is a key to the future multiple-thickness gate oxide technology.

References

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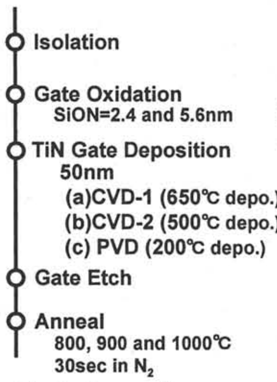

Fig.1. Process flow.

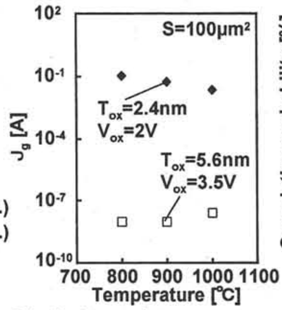

Fig.2. Anneal temperature dependence of the J_g. V_{ox} is defined as V_g-V_{fb}.

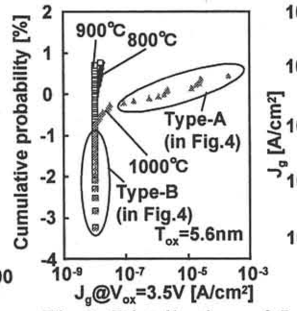

Fig.3. Distribution of J_g after 800, 900 and 1000°C anneal.

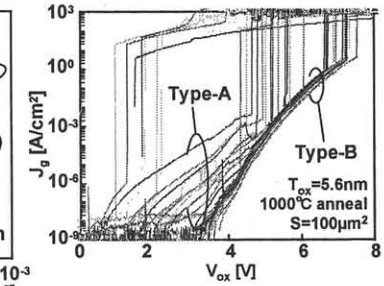

Fig.4. J_g-V_{ox} characteristics of the thick oxide capacitor after 1000°C anneal. Observed J_g can be categorized into two groups (type-A, B).

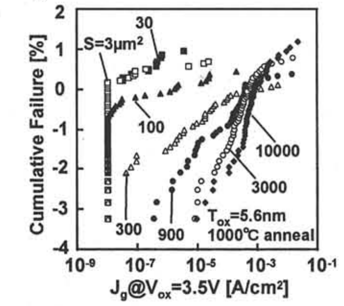

Fig.5. Capacitor area dependence of the J_g distribution for CVD-1 gate samples with thick oxide.

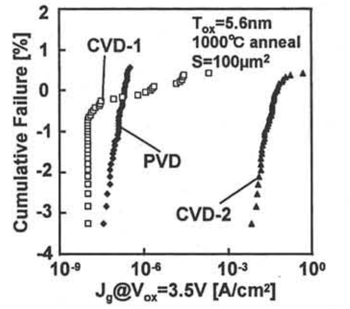

Fig.6. Process dependence of the J_g distribution.

Table I. Composition of the TiN films. Significant difference is observed in residual Cl concentration.

		Ti [at%]	N [at%]	Cl [at%]	x in TiNx
CVD-1 (650℃)	as depo.	47.9	46.7	1.77	0.97
	RTA	48.6	45.7	1.09	0.94
CVD-2 (500℃)	as depo.	48.2	46.3	4.16	0.96
	RTA	46.4	43.4	1.54	0.94
PVD	as depo.	48.7	42.3	0.01	0.87
	RTA	47.1	42.9	0.12	0.91

RTA : 1000℃10sec

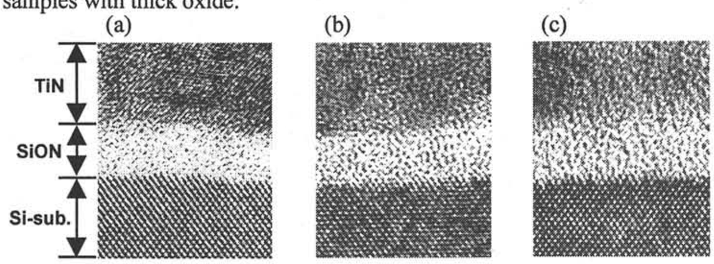

Fig.7. Cross sectional TEM images of TiN gate MOS capacitors after 1000°C anneal. (a) CVD-1, (b) CVD-2, (c) PVD. No reaction of Ti with SiON was observed at TiN/SiON interface for each sample.

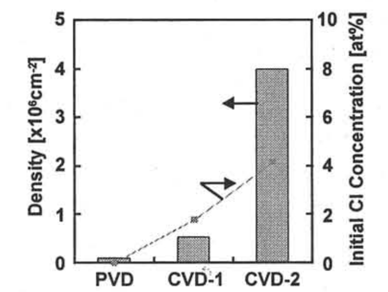

Fig.8. Correlation betweeñ th density of weak spots and residual Cl concentration.

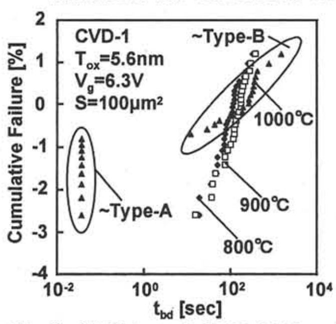

Fig.9. CVS-t_{bd} of CVD-TiN gate MOS capacitor. *Weibull distribution for 1000°C annealed sample has two components, corresponding to the type-A and type-B in Fig. 4.*

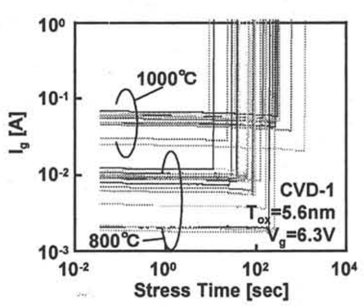

Fig.10. Stress time dependence of I_g for the type-B. The t_{bd} distribution of 1000°C anneal sample slightly increased as compared to that of 800°C sample.

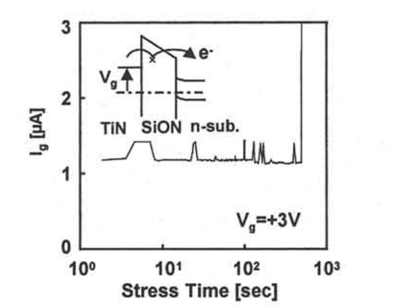

Fig.11. Stress time dependence of I_g for the type-A. Current fluctuations before hard breakdown during the stress is considered to the electron conduction through Cl-related trap site [10].