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Etch Damage of n$^+$Poly-Si Gate Side Wall as Evaluated by Gate Tunnel Leakage Current

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1. Introduction

Significantly high performance of n-MOSFETs with 1.5-2.0nm thick gate oxides and 40-100nm gate lengths has been reported[1-3]. The transconductance enhancement for 40nm gate length nMOSFETs has been limited by 30% as compared to the case of 100nm transistors because of the parasitic resistances and the carrier velocity saturation[4]. This paper describes the influence of plasma induced damage of n$^+$poly-Si gate side walls on the performance of MOSFET with 1.86nm thick gate oxides and 30nm-20μm gate lengths.

2. Results and Discussion

nMOSFETs with 1.86nm thick gate oxides and 30nm-20μm gate length were fabricated. The gate resist pattern with EB lithography was transferred to an SiO_2 layer on the n$^+$poly Si layer by RIE. Subsequently the SiO_2 was shrunk by chemical etching with 0.5% dilute HF. Precise control of mask shrinking down to 30nm was achieved. Phosphorous doped n$^+$poly-Si gate etch was performed by an ECR etcher in which a Cl_2/N_2 gas mixture was employed for the anisotropic etch at a pressure of 5mTorr with a self-bias of 84V. The etching gas was changed from Cl_2/N_2 to Cl_2/O_2 just before the etch end point in order to improve the selectivity of poly-Si to SiO_2 up to 400. The cross sectional SEM image of etched n$^+$poly-Si gate pattern is shown in Fig. 1, where the gate length is 30nm. The thermal budget after gate fabrication was 750°C, 30min for SiO_2 deposition as an implantation cap and 850°C, 30min for source/drain junction formation.

Figure 2 shows the gate current versus gate voltage characteristics for different gate lengths. The direct tunnel currents at $V_g=\pm 2.5$V are plotted as a function of gate length as shown in Fig. 3. Since the gate width W_g is kept constant at 10μm, the gate current should be proportional to the gate length. However, in the sub-0.5μm gate length region the gate current significantly decreases, deviating from $|I_g| \propto L_g$ curve. This current decrease occurs at both polarities of gate bias. As seen in Fig. 3 at Lg<0.5μm the hypothetical gate current in proportion to gate length(dashed line) is compared with the measured current and the apparent gate length difference ΔL_g shown in the figure is plotted as a function of L_g in Fig. 4, where ΔL_g=100nm is obtained regardless gate bias polarity. Assuming that the gate current reduction is induced by the decrease of conductive gate area by $W_g \times \Delta L_g$, it is likely that the gate side wall resistance is considerably high. We measured the gate length dependence of gate resistance as shown in Fig. 5. In the sub-0.5μm gate length region, the gate resistance significantly deviates from the relationship $R_g \propto L_g^{-1}$. This is consistent with the results of Figs. 3 and 4 in which the resistance of poly-Si side walls is significantly high. Figure 5 also represents in-depth profile of electron density plotted from the gate side wall surface to the bulk obtained from the measured gate length dependence of R_{poly}. The gate length dependence of poly-Si resistance is changed by changing the thermal budget after gate etch as indicated in Fig. 6. The poly-Si side wall damage due to ion implantation is negligible because a cap oxide(HTO) is deposited just before ion implantation. Therefore, it is likely that the pile-up of phosphorous atoms at the CVDSiO_2/poly-Si interface is enhanced by the remaining side wall damage, and thus the phosphorous concentration in poly-Si tends to deplete as the gate length becomes shorter than 0.5μm because the ratio of pile-up phosphorus atoms at the SiO_2/poly-Si interface to the total number of phosphorus atoms in poly-Si gate becomes larger for Lg<0.5μm. Based on the carrier concentration profile shown in Fig. 5, the potential profile in the gate can be calculated if it is assumed that the carrier concentration at the poly-Si surface layer is intrinsic due to remaining defects, the depletion layer in the both side of the gate is generated as shown in Fig. 7. The gate side walls should be highly resistive as a result of reduction of total impurity content in the gate because of damage enhanced phosphorus pile-up[5]. The gate voltage is not efficiently applied to the oxide under the gate side wall layer, resulting in the gate current reduction. In fact as shown in Fig. 2 the gate current observed at gate voltages between 0V to -1V is direct tunneling current from the n$^+$poly-Si gate to the source/drain

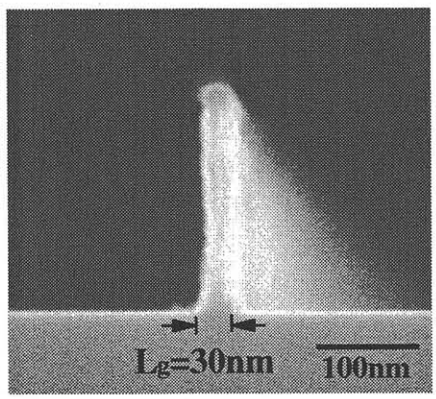

Fig. 1. 30nm n$^+$poly-Si gate etch pattern.

extension and the gate current should not depend on gate length. However, the gate current depends on gate length because the increase of the gate side wall resistance or band bending interrupts the tunneling from the gate to the source/drain extension. Also the gate/extension overlap is electronically insufficient even though physical source/drain overlap is enough. Therefore the series resistance of MOSFETs is increased and transconductance is reduced. The measured transconductance for 0.1μm MOSFETs is 450mS/mm which is about one half of the expected value by simulation while for 30nm MOSFETs Gm= 435mS/mm which is not improved with respect to that of 0.1μm MOSFET. It is also important to note that the parasitic resistances in the source/drain region deteriorate Gm because the salicide technology was not employed.

3. Conclusion

The phosphorus pile-up at the n^+poly-Si side wall/SiO_2 interface is enhanced by remaining ion-induced damage in side wall layer. This reduces the total number of phosphorous atoms in poly-Si at sub-0.5μm gate lengths. The gate/extension overlap is electronically insufficient even though the physical source/drain overlap is enough because of the depletion layer in the side wall surface region. Therefore the series resistance of MOSFETs is increased and hence transconductance is reduced.

Acknowledgment

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References

[1]M. Ono et al., IEEE IEDM p.119, 1993.

[2]G. Timp et al., IEEE IEDM p.930, 1997.

[3]Q. Xiang et al., IEEE Symposium on VLSI Digest of Technical Papers p.160, 1998.

[4]H. S. Momose et al., IEEE IEDM p.593, 1994.

[5]K. Morino et al., Ext. Abst. of 1997 Int. Conf. on SSDM(1997)p. 18.

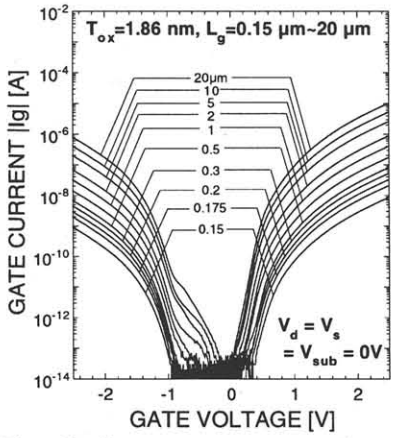

Fig. 2. Gate current-gate voltage characteristics of fabricated nMOSFETs.

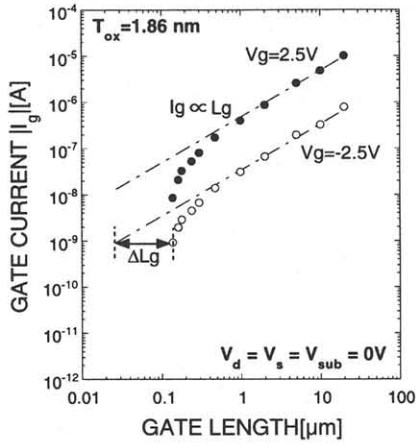

Fig. 3. Gate length dependence of I_g.

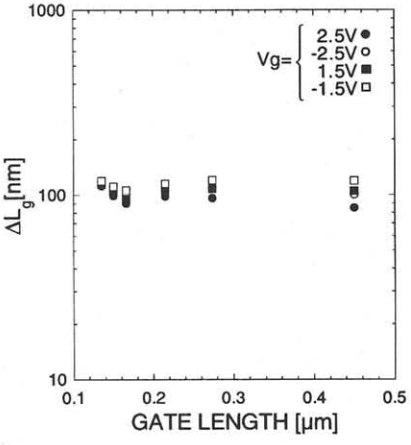

Fig. 4. ΔL_g vs. L_g for different V_g.

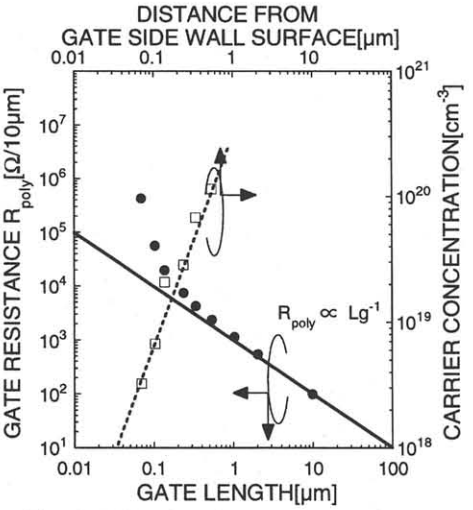

Fig. 5. Gate length dependence of gate resistance R_{poly} and carrier profile in poly-Si gate.

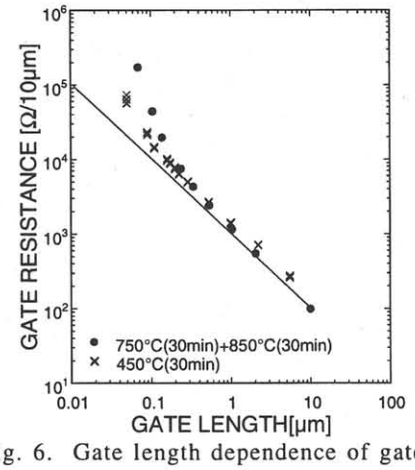

Fig. 6. Gate length dependence of gate resistance for different thermal budget after gate etching.

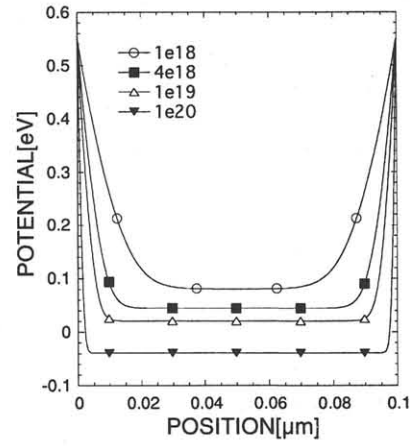

Fig. 7. Potential distribution for different bulk carrier concentrations from $1x10^{20}$ to $1x10^{18}$ cm^{-3} for the gate length of 0.1μm (Fermi level corresponds to zero potential).