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# Low-Temperature Selective Deposition of Silicon by Time-Modulation Exposure of Disilane and Formation of Silicon Nanowires

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## 1. Introduction

The selective deposition technique has a big potential to fabricate very narrow width structures. We have been studying a selective atomic-layer deposition of silicon nitride on silicon and no deposition on $SiO_2$ [1-2]. When the selective deposition of Si on silicon nitride and no deposition on $SiO_2$ is achieved, very narrow Si wires separated by the silicon nitride films can be integrated as shown in Fig.1. The Si and silicon nitride films are alternately deposited on the sidewall of the $SiO_2$/(Si or silicon nitride)/$SiO_2$ stacked structures.

In this paper we report a new method for the low-temperature (410°C) selective deposition of Si on silicon nitride. Very narrow (21nm width) Si wires have been fabricated using the selective deposition and the electrical properties have been evaluated. The resistivity of the Si wires fabricated by the selective deposition is much smaller than that fabricated by the conventional reactive ion etching (RIE). This technique is applicable to the formation of poly-Si gate with small resistivity for the high-performance ultrasmall MOS transistors and quantum effect devices.

## 2. Selective Deposition of Si

The low-temperature selective deposition of Si was achieved at 410°C by the time-modulation exposure of disilane ($Si_2H_6$), while the previous selective deposition temperature between $SiO_2$ and silicon nitride ($Si_3N_4$) was ~950°C [3]. The $Si_2H_6$ gas is periodically admitted into the quartz chamber with an adequate interval time as shown in Fig. 2. There exists an incubation time before starting the film growth [4]. We have utilized the incubation-time difference depending on the substrate material to the selective deposition. In the continuous gas exposure, the film thickness of the selective deposition is limited by the incubation time. Whereas the thickness limitation is significantly relieved by using the intermittent exposure of the source gas, since the substrate surface condition may approach to the initial condition by the desorption of the adsorbed species during the vacuum evacuation.

The temperature dependence of the deposition rate of Si on thermal $SiO_2$ and $Si_3N_4$ deposited by a chemical vapor deposition using $SiH_2Cl_2$ and $NH_3$ at 750°C is shown in Fig. 3. The both substrate surfaces were treated in the diluted HF followed by deionized water rinse for 1 min. Therefore, the $SiO_2$ surface is O-H terminated [5], while the bonded hydrogen does not exist on the $Si_3N_4$ surface [1] which was verified by the Fourier transform infrared attenuated total reflection (FT-IR-ATR) spectroscopy. The selective deposition of Si on $Si_3N_4$ surface with small amount of deposition on $SiO_2$ is achieved in the two growth conditions. One is the high-temperature (>580°C) and low-pressure ($10^{-5}$ Torr) condition and another is the low-temperature (<500°C) and high-pressure ($10^{-3}$ Torr) condition. The mechanism for the selective growth at the high-temperature and low-pressure region must be the reaction, $Si+SiO_2 \rightarrow 2SiO$ (with high vapor pressure) [6]. The activation energy of 2.1 eV observed in Fig. 3 well fit to that of thermal dissociation of $Si_2H_6$ [7]. The enhanced growth rate on $Si_3N_4$ at the low-temperature and high-pressure region may be due to the short incubation time on $Si_3N_4$ compared with that on $SiO_2$ [4].

The Si selective deposition was carried out on the $SiO_2/Si_3N_4/SiO_2$ sidewall fabricated by RIE. Figure 4 shows the cross sectional scanning electron microscope (SEM) images for different growth conditions. The Si nanowires of ~30nm width are formed on the sidewall of $Si_3N_4$ at the high-temperature, low-pressure and at the low-temperature, high-pressure conditions. On the other hand, in the medium-pressure condition ($10^{-4}$ Torr, 600°C), the Si film is conformably deposited on the whole surface.

## 3. Si Nanowires and Electrical Properties

The Si nanowires were fabricated under the low-temperature (410°C) condition because of its smaller surface roughness than that grown at the high-temperature condition. The fabrication procedure of the Si nanowires is shown in Fig. 5 (a)-(c). Thin Si films grown on $SiO_2$ is removed by the chemical dry etching using remote microwave plasma of $CF_4+O_2$. The 21nm width x 28nm thick Si nanowires were fabricated. The size of the wire was measured by the SEM. The phosphorous doping was carried out using $POCl_3$ at 850°C. The passivation layer formation (non-doped and phosphorous doped silicate glass, both 300nm thick), the contact hole formation by the wet etching, the Al film deposition by the sputtering, the lithography, and the wet etching were carried out. Finally, the sample was annealed at 450°C to reduce the contact resistance. The optical microscope photograph of the sample is shown in Fig. 5 (d).

Figure 6(a) shows the current-voltage (I-V) curves for the fabricated Si nanowires, which indicates the linear I-V relationship. The length dependence of the resistance of the Si nanowires is plotted in Fig. 6(b), from which the resistivity of the Si wires is calculated. The result is summarized in Table I with the data for the Si wires fabricated by the RIE. For the selective deposition sample, the resistivity is about 1/5 times that of the RIE sample, even though the phosphorous is more heavily doped and the size is larger for the RIE sample. The resistivity increase for the RIE sample may be due to the plasma-induced damage at the etched sidewall of the Si wire during the RIE. On the other hand, the Si wires fabricated by the selective deposition has no plasma damage, resulting in the good conductivity.

## 4. Conclusion

A new low-temperature (410°C) selective deposition method for Si, "time-modulation exposure method", was developed. The Si nanowires with the size of 21nm width x 28nm thick were fabricated by the selective deposition. They have a larger conductance than that fabricated by the RIE. This technology is useful for fabrication of the poly-Si gate with small resistivity for the ultrasmall transistors and quantum effect devices.

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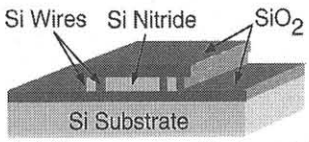



Fig. 1 Integrated Si nanowires fabricated by the selective deposition of Si and silicon nitride.

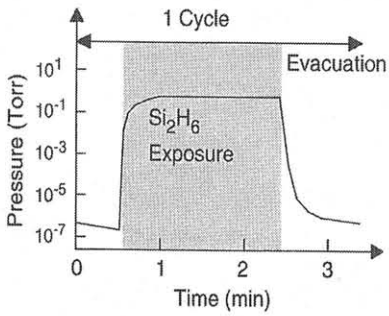
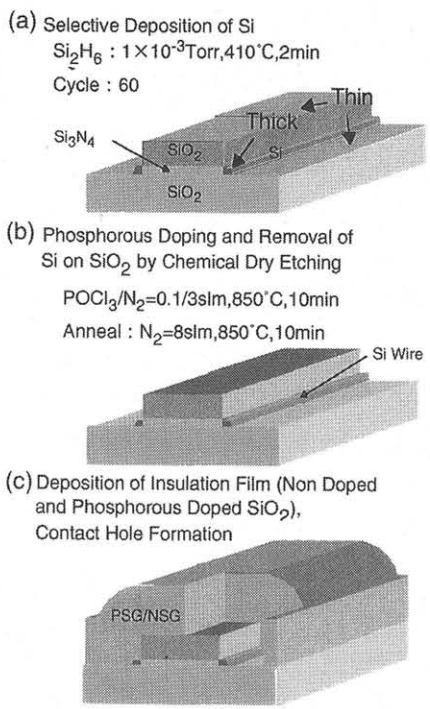



Fig. 2 Pressure vs time for the modulation exposure method.



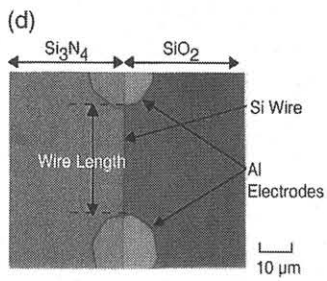




Fig. 5 (a)-(c) Fabrication procedure of Si nanowires and (d) optical micrograph of the fabricated sample.

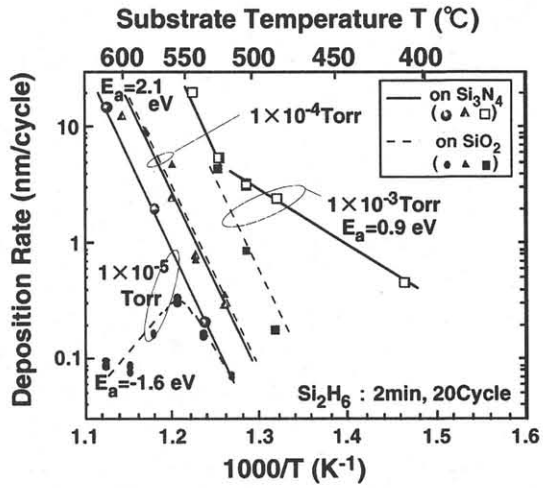



Fig. 3 Temperature dependence of the deposition rate of Si on $SiO_2$ and $Si_3N_4$.

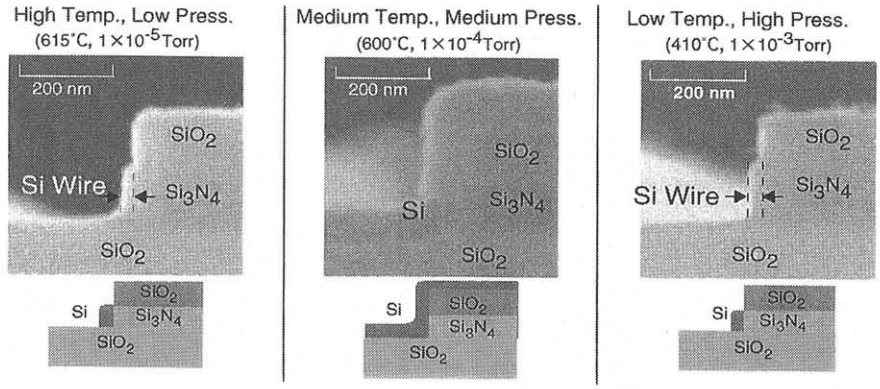



Fig. 4 Cross sectional SEM images for diffrent growth conditions. The bottom figures indicate the schematic of the structures.

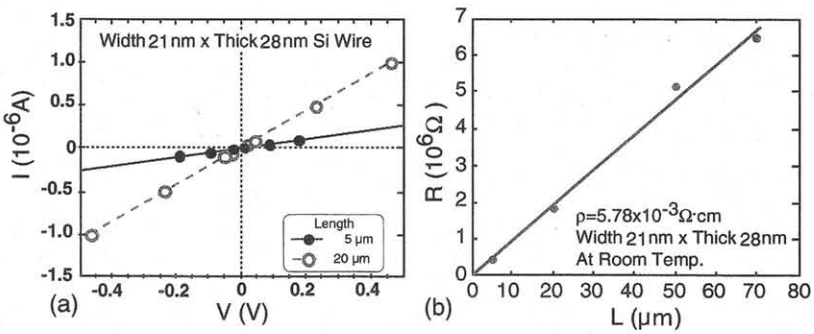



Fig. 6 (a) Current-voltage (I-V) curves for Si nanowires of 21nm width x 28nm thick and (b) length dependence of the resistance of the Si nanowires.

Table I Comparison between RIE (plasma etching) and selective deposition samples.

| Method | Plasma Etching | Selective Deposition |
|---|---|---|
| Size (nm×nm) | 70×220 | 21×28 |
| Resistivity (Ω·cm) | 2.6×10$^{-2}$ | 5.8×10$^{-3}$ |
| Phosphorous Doping | 850°C, 30min | 850°C, 10min |
| Anneal | 850°C,10min | |