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Ultra Shallow Junction Formation for 80 nm CMOS by Controlling Transient Enhanced Diffusion

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1. Introduction

When MOSFET dimensions are reduced, from the viewpoints of durability of short channel effect (SCE) and reduction of parasitic resistance, ultra shallow and steep junction is more desired. Recently, novel process sequences are reported such as source/drain junction formation prior to extension formation in order to minify thermal budget for ultra shallow junction (USJ) [1]-[3]. These process sequences, however, contain several difficulties or concern in the sight of mass production such as compatibility with SALICIDE process (especially thermal durability of $CoSi_2$), boron penetration through thin gate insulator (BP) from prior-doped gate electrodes during USJ formation thermal budget. Moreover, even in these processes, damage recovery and activation anneal of extensions are indispensable and should be optimized. Thus, understanding and controlling of transient enhanced diffusion (TED) are quite essential for USJ formation.

For the sake of low sheet resistance and spreading resistance, high dose implantation for extensions of source/drain junctions is indispensable. This condition increases TED induced by point defects. On the other hand, novel anneal process such as spike anneal or excimer laser light thermal process has developed [4]-[5]. These annealing processes seem to be promising candidates for USJ formation. These processes, however, use totally different apparatuses from conventional RTA, and need a high level of controllability such as millisecond order thermal profile control or surface treatments for laser light absorption.

In this paper, process dependence on short channel effect is presented experimentally and optimization of damage recovery annealing sequence (DRA) by utilizing conventional RTP system is proposed to overcome this problem.

2. Device Fabrication

The process sequences of experiment with Co salicided CMOS technology are shown in Fig. 1. CMOSFETs with physical gate length down to 60 nm and with 2.5nm physical gate oxide thickness were fabricated by using 110 nm CMOS logic process integration technology. Before LPCVD SiN layer deposition for sidewall, shallow extension formation using low energy ion implantation as 2-5 keV BF_2^+, As^+ for p- and nMOSFET, respectively, and damage recovery RTA (DRA) of 750-1000°C for 5-30 s were performed. Three kinds of sequence for damage recovery were examined in this work. Sequence "A" as shown in Fig.1, contained simultaneous DRA for n-, p-extension implantation. In the sequence "B", in the meanwhile, samples received different temperature DRA for n-, p extension, separately. Sequence "C" is very similar to sequence "A" except Ge PAI before p-extension implantation. After sidewall formation, n^+/p^+ doping of gate and diffusion and activation RTA (A-RTA) of 1000°C for 10 s were performed. Samples were sequentially received Co SALICIDE process.

3. Damage Recovery RTA for USJ

As-implanted arsenic profile was steep such as 20 nm at the concentration of $1x10^{18}$ cm^{-3}. Profile after 800°C RTA just behind ion implantation was almost the same as as-implanted profile for arsenic as shown in Fig. 2. In the case of arsenic, however, very fast diffusion occurred during SiN LPCVD for sidewall formation at the temperature of 700°C. Arsenic profile received high temperature DRA is steeper than that of low temperature DRA as shown in Fig. 3. Short channel effect was also improved by around 900°C DRA as shown in Fig. 4(a). In contrast to arsenic case, lower temperature DRA is preferable for boron. In boron case, thermal diffusion (TD) is more prominent than TED. It was recognized that only the samples received DRA of 960°C showed severe threshold voltage roll-off as shown in Fig.4 (b). Dependence of overlap capacitance (C_{ov}) on DRA temperature consists with SIMS profile and threshold voltage roll-off characteristics of MOSFET. C_{ov} of nMOSFET has minimum at 900-950°C as shown in Fig. 5(a). On the contrary, C_{ov} of pMOSFET increased rapidly over 850°C as shown in Fig. 5(a).

Independence of drive current vs. off-state leakage current characteristics from DRA temperature as shown in Fig. 6 means that DRA temperature dependence of threshold voltage roll-off attributes to lateral diffusion of extension that modulates effective channel length rather than 2D profile of extension. Therefore, simultaneous DRA sequence "A" as shown in Fig. 1 is not appropriate for DRA process. For USJ formation, samples should receive higher temperature DRA (DRA-1, 900-950°C) after n-extension implantation and lower temperature DRA (DRA-2, 750-800°C) for p-extension implantation in sequence. In the case of using Ge pre-amorphization (PAI), a threshold voltage roll-off characteristic is greatly improved as shown in Fig. 7. TED is, however, the dominant factor below 900°C shown as Fig. 5(b) even though the case of p-extension. C_{ov} of Ge PAI pMOSFET remains smaller than that of no-PAI samples as shown in the Fig. 5(b). It is speculated that diffusion of boron was retarded by Ge PAI. Therefore, it is experimentally found that p- and n-extension DRA could be summed up into one DRA as shown in Fig.1 sequence "C" owing to using Ge PAI. After optimization DRA, temperature dependence of TED during SiN LPCVD process was investigated. There was very little dependence on deposition temperature observed as shown in Fig. 8. Therefore, optimized DRA enables to prevent TED and make ultra shallow junction.

4. Conclusion

Damage recovery process sequence of source/drain extension was investigated by experimentally from the viewpoint of short channel effect immunity. Optimized damage removal anneal temperature is totally different for n, pMOSFET, respectively. Using Ge pre-amorphization prior to p-extension implantation, these RTA can be summed up to onetime and cut raw process time without causing degradation of short channel effects.

References

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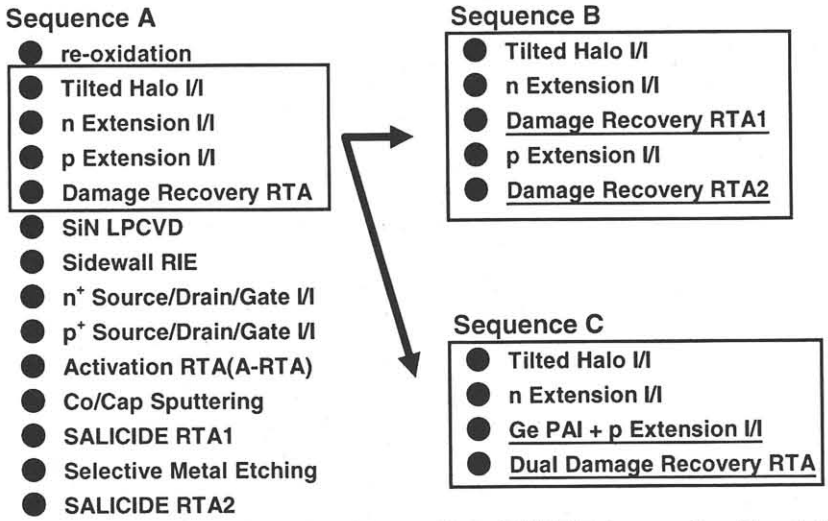


Fig. 1 Process sequences of CMOS technology with Co SALICIDE. Sequence B or C is substituted for boxed process module of sequence A.

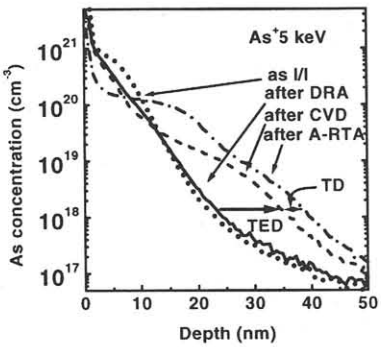


Fig. 2 Arsenic profile evolution from as-implanted to final activation RTA for the case of DRA temperature of 800°C.

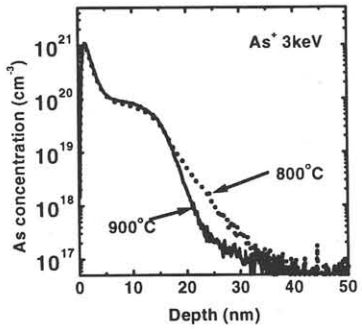
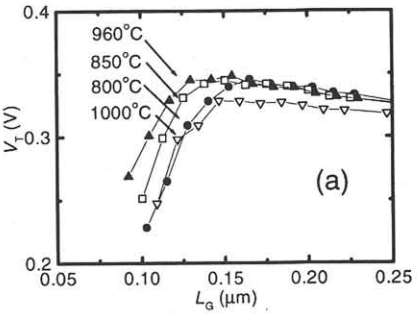


Fig. 3 Dependence of arsenic profile after activation RTA on DRA temperature.



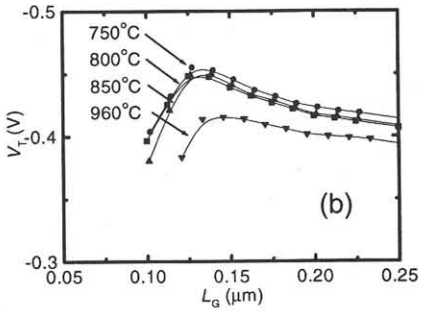
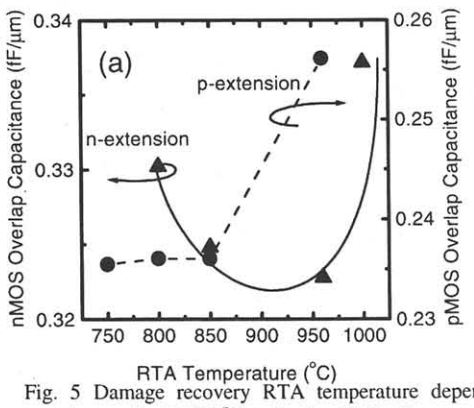


Fig. 4 DRA temperature dependence on Vth roll-off. For nMOSFET, higher DRA is preferable shown as (a). On the contrary, lower temperature is preferable for pMOSFET shown as (b).



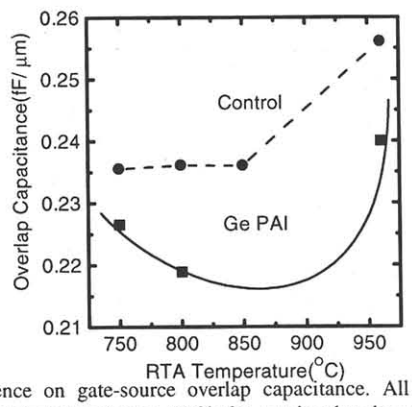
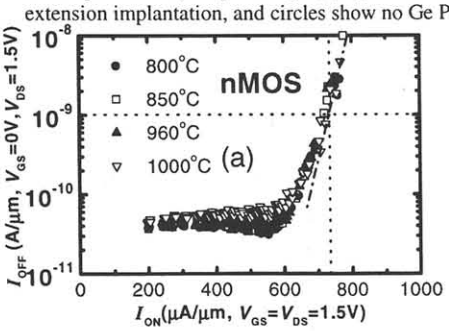


Fig. 5 Damage recovery RTA temperature dependence on gate-source overlap capacitance. All samples received 1015°C activation RTA after source/drain implantation. (a)Circles or triangles show n- or pMOSFET, respectively. (b)Squares shows pMOSFETs that received Ge PAI prior to p-extension implantation, and circles show no Ge PAI pMOSFETs.



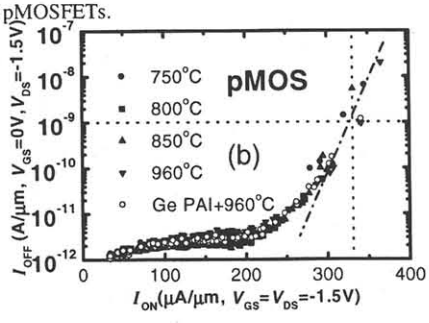


Fig. 6 Damage recovery RTA temperature dependence on I_{on}-I_{off} characteristics.

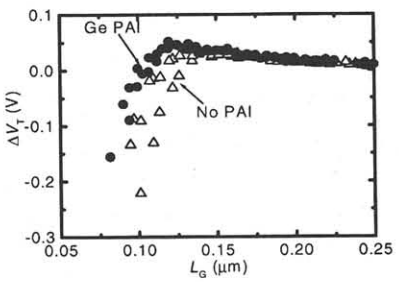


Fig.7 Impact of Ge PAI in the case of 960°C DRA. Filled symbols show PAI samples and open symbols show no PAI samples.

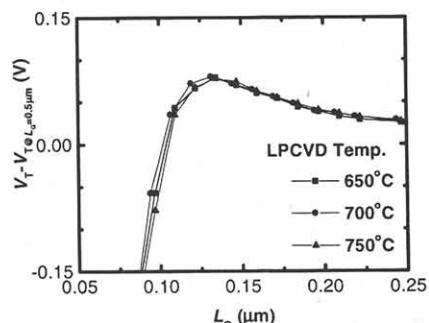


Fig.8 SiN LPCVD temperature dependence of nMOSFET Vt roll-off. All samples received 900°C DRA.