Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 406-407

A-7-4

Ultra-Shallow and Low-Leakage p^+n Junctions Formation by Plasma Immersion Ion Implantation (PIII) and Low-Temperature Post-Implantation Annealing

Kei Kanemoto,[1] Herzl Aharoni,[2,*] and Tadahiro Ohmi[2]
[1]Department of Electronic Engineering, Graduate School of Engineering, Tohoku University,
05 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-217-7122 / Fax: +81-22-224-2549, E-mail: kanemoto@sse.ecei.tohoku.ac.jp
[2]New Industry Creation Hatchery Center, Tohoku University,Aza-Aoba, Aramaki, Aobaku Sendai 980-8579, Japan
* At leave from the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva, 84105, Israel

1. Introduction

Continuous scaling-down of MOSFET in ULSI (ultra large scale integration) systems requires shallower source/drain junctions. To meet this requirement, acceleration energy must be considerably decreased. Conventional ion implantation equipment presents a problem in this respect. Lowering the beam energy is accompanied by a reduction of beam current, a fact that significantly prolong the implantation time reducing the throughput, a fact which make it commercially prohibited. On the other hand, plasma immersion ion implantation (PIII), in which wafer is placed directly in a plasma, is receiving more and more attention for its very high ion current capability, very low implantation energy, smaller size of equipment, simple structure, etc. Although there have been several reports that show good junction characteristics achieved by PIII followed by high-temperature post-implantation annealing [1-3], any reports on low-temperature post-implantation annealing has not been made. Lowering process temperature is an essential requirement for future ULSI devices.

The purpose of this work is to present the characteristics of junctions formed by BF_3 PIII using parallel-plate type plasma and a range of low-temperature post-implantation annealing. Very low-leakage currents (~10^{-11} A at −1 V, 1-mm-sq. diode) and ultra-shallow junctions have been formed by the low-energy implantation and low-temperature post-implantation annealing. The results obtained are comparable to junctions made by the state of the art conventional ion implantation equipment.

2. Parallel-Plate Type Plasma Chamber

For PIII experiments, we use a plasma chamber, which has two parallel-plate electrodes. The upper one is connected to the ground and the lower one is connected to RF power supply (13.56 MHz) through RF matching network. The sample substrate is placed on the lower electrode (RF electrode). When RF power is applied, plasma is formed and large negative voltage (self-bias) appears on the RF electrode. Due to this self-bias, positive-charged ions in the plasma are accelerated via the plasma sheath and then implanted into the substrate. Since no DC current needs to flow through the sample wafer, this technique can be applied even to SOI wafers. Implantation dose is controlled by implantation time and constant current. The top surface of RF electrode is covered with shielding silicon wafer and the substrate is placed upon it to suppress metallic contamination caused by sputtering of RF electrode. As a result, metallic contamination level is reduced to a level of 10^{10} atom/cm^2 (determined by TRXRF) measured on the implanted substrate after ~10^{15} cm^{-2} implantation and following wet cleaning (SPM: $H_2SO_4 + H_2O_2$, DHF: 1% HF).

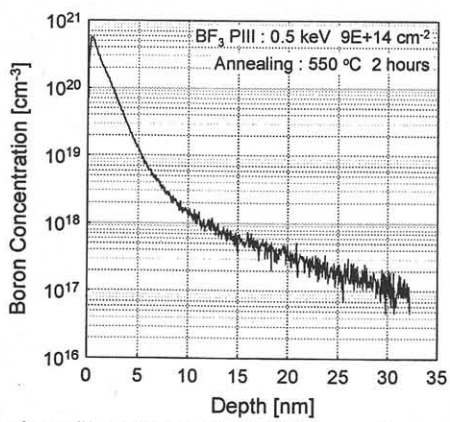

Fig. 1 Depth profile of boron after 550 °C annealing measured by SIMS.

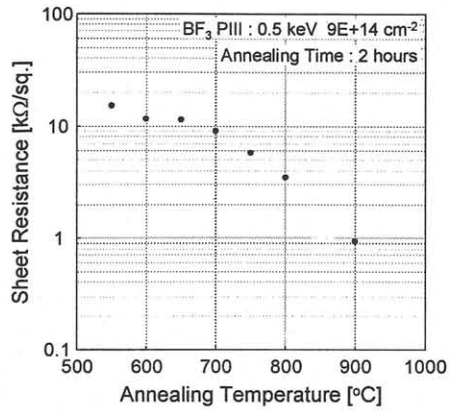

Fig. 2 Sheet resistance of BF_3 PIII layer plotted as a function of annealing temperature.

3. Experimental

n-type (100), ρ~40 Ωcm, Cz silicon wafers (33 mm ϕ) were implanted using 100% BF_3 plasma by PIII. The implantation energy and dose were 0.5 keV and 9×10^{14} cm^{-2}, respectively. The implantation time was 1 sec, a fact which demonstrates the potential for high throughput industrial process, in comparison to the long conventional implantation times. Then the samples were annealed at temperatures raging from 550 °C to 900 °C in Ar ambient for 2 hours. Before and after PIII, wet cleaning (SPM, DHF) is carried out.

4. Results and Discussion

Figure 1 shows the depth profile of boron after 550 °C-annealing measured by SIMS. According to the very low implantation energy of 0.5 keV, the penetration depth of boron is very shallow. Boron atoms deeper than amorphous/crystalline interface are hardly activated by low-temperature annealing [4].

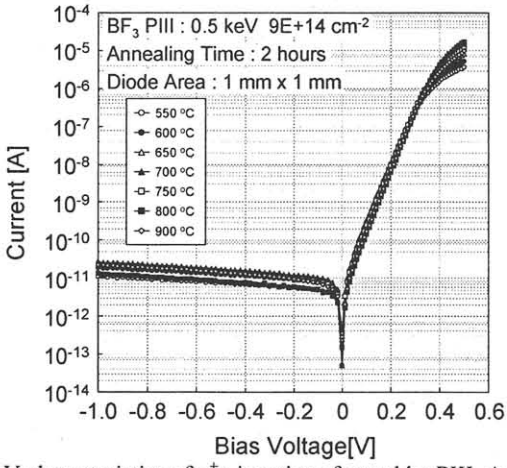

Fig. 3 I-V characteristics of p^+n junctions formed by PIII. Annealing temperature is 550-900 °C. Diode area is 1 mm × 1 mm.

Accordingly, the electrical junction depth may be even less than metallurgical junction depth. **Figure 2** shows the sheet resistance (R_s) of PIII layer after 2-hours annealing plotted as a function of annealing temperature. Strong dependence of R_s is seen. In low-temperature, where no boron diffusion occurs, R_s exceeds 10 kΩ/sq. High value of R_s is expected in shallow junctions. However, the value indicates that the dopant activation is not high. Nevertheless the obtained junction characteristics are comparable to those made by conventional implantation [4]. **Figure 3** shows the I-V characteristics of 1 mm × 1 mm diodes made at various annealing temperatures. Measurements were performed at 300 K. The characteristics are very good and there is only a little dependence on annealing temperature. At about 0.4 V in forward bias, the current starts to deviate from exponential curve. This would be due to large sheet resistance and contact resistance. In **Fig. 4**, leakage current at reverse bias of 1 V is plotted as a function of annealing temperature. For all temperatures, very low leakage current in the range of ~10-11 A is obtained. Also, good n-values which ranged from 1.03 to 1.12 for various annealing temperatures were obtained (**Fig. 5**). **Figure 6** shows the ratio of peripheral current (I_P) to area current (I_A) plotted as a function of annealing temperature. I_P and I_A were calculated for 400 μm × 400 μm diode using peripheral current density (J_P) and area current density (J_A) obtained by measuring comb-shaped diodes which have same area (A = 0.16 mm^2) but different peripheral length (L = 1.6-6.4 mm). It can be seen that I_P/I_A increases with the decrease of annealing temperature.

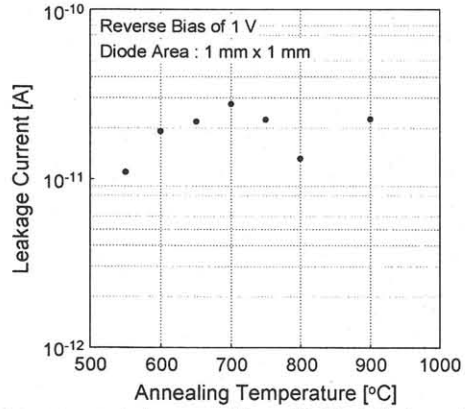

Fig. 4 Leakage current at reverse bias of 1 V plotted as a function of annealing temperature. Diode area is 1 mm × 1 mm.

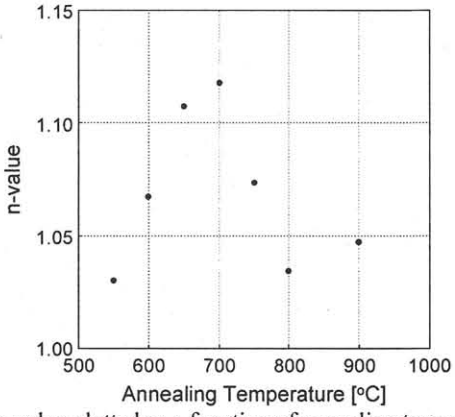

Fig. 5 n-value plotted as a function of annealing temperature.

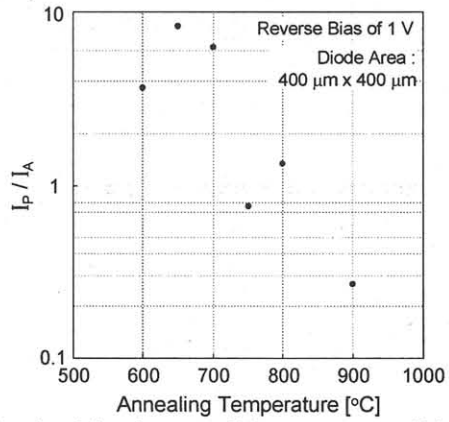

Fig. 6 Ratio of peripheral current (I_P) to area current (I_A) for 400 μm × 400 μm diode plotted as a function of annealing temperature.

I_P/I_A reaches a value of about 10 at 650 °C, which means 90% of total current flows peripherally. This would be caused by high electric field at the junction periphery due to the high curvature resulting from its shallowness at the corner of p^+ region. In high temperatures, the curvature at the periphery becomes smaller due to deeper junction resulting in weaker electric field there and smaller I_P/I_A. Accordingly, high I_P/I_A is to be expected as an inherent effect in all future ULSI shallow junctions.

5. Conclusion

Very low-leakage current (~10^{-11} A at –1 V, 1-mm-sq. diode) and ultra-shallow p^+n junction has been formed by BF_3 PIII using parallel-plate type plasma and low-temperature (550 °C) post-implantation annealing. The technology for higher dopant activation is pursued by us for further junction performance improvement.

Acknowledgments

This study was carried out in Super Clean Room of the Laboratory for Electronic Intelligent Systems, Research Institute of Electrical Communication, Tohoku University.

References

[1] X. Y. Qian et al., Appl. Phys. Lett., **59**, pp. 348 (1991).

[2] E. C. Jones and N. W. Cheung, IEEE Electron Device Lett., **14**, pp. 444 (1993).

[3] C. Chan and S. Qin, Microelectron. Reliability, **38**, pp. 1485 (1998).

[4] A. Nakada et al., J. Appl. Phys., **81**, pp. 2560 (1997).