

A-8-1 (Invited)

Current State of Research and Development for Electronic System Integration

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1. Introduction

Higher performance of electronic system operation has been demanded day by day. However, electronics packaging is now the bottle neck to extract the full performance of high CPU operation. The following new project of "the Ultra High-Density Electronic System Integration (E-SI)" of ASET are started from April 1999 with 18 companies' researcher.

This 5-year Project activity is mainly sponsored by MITI and through the New Energy Development Organization (NEDO). There are many activities outside of Japan for the basic technology leadership in the next industrial and academic research area of electronics System Integration. For the future electronics industry it's quite important to understand the future products needs, the technology trend and the social dynamic changing such a seamless information exchanging by light weight and easy handling, portable, clear and vivid visual panel, easy voice controlling, low power consumption, low price, safety security etc. Because the world has been highly intellectualized, safeguarded and politically stabilized, people feels significance of information technology. At the same time high-speed processing accuracy, reliability and saving energy are required to protect the global environment. And it creates the new seamless telecommunication value added society and multi media communication. For these system needs the future system circuit and controlling architecture should be divided and reconstructed into the most optimum subsystem.

Then the suitable subsystem circuit will appear with the maximum performance. This situation should be clear for the future Electronics System Integration by the top down designing. The right and optimum consideration for combining the electronics and electro-magnetic circuit, optic and electro-optics, actual mechanical production engineering and other system controlling technology will support those technology installation with the total designing. This paper is the first FY activity report of E-SI contained the main target items and the E-SI technology trend researching.

2. The system technology trend and needs for E-SI

Technology trend

- Minimizing and the lightest weight.
- High performance with low power consumption.
- Digital processing and networking by smooth communication connection
- Huge information memory data and its data processing and ultra high speed instruction / transfer.
- Electronics and opto-electronics technology development.
- Total system designing and packaging under the high quality production.
- Minimum energy consumption, EMI / EMC consideration.
- Easy testing, easy repairing and maintenance.

E-SI Project Target Item (Needs for E-SI)

The national project for this Ultra High-Density Electronic System Integration basic technology researching target are the followings.

1. Super-high-density three-dimensional LSI chip Integration technology: (High density 3D stacked Integration)

Table I Super-high Density E-SI Researching Plan

R&D Term	FY 1999	FY 2000	FY 2002	FY 2003	FY 2004
① Super High-Dens. 3D Chip Integration Tech.	LSI Chip Stack Forming Process Technology		Try & evaluation by through-process		
	Stacking, Bonding, Test Basic Tech.				
② Opto-Electronic Packaging	Opto-Elec. Elemental Parts trial sample Evaluation		Model sample Evaluation		Total Evaluation
	Find out improved matter for OPTO-3D				
③ Optimum Circuit & Structure Design	EMI evaluation System Develop.& Test		EMI generator LSI Design & Analyzing its		Wrap-up
④ Market &Tech. Trend	Technology trend & New Market Survey				

- Stacked LSIs with through Holes (less than 10 μ m diameter and 50 μ m depth) in Si substrate.
 - The LSI chip will be connected with micro-bumps on the each chip (DRAM & CPU).
2. Opto - electronics hybrid integration technology:
- LSIs with LEDs on the board (mother and daughter-board) with the optical interconnection instead of metal.
 - Higher performance of chip to chip will be realized by optical and electronic interconnection technology.
3. Optimum circuit design technology for 3-D and opto-electronics interconnection:
- Solution providing for especially Electro Magnetic Compatibility(EMC) problem for 3-D and opto-electronics interconnection

Relationship between Subjects

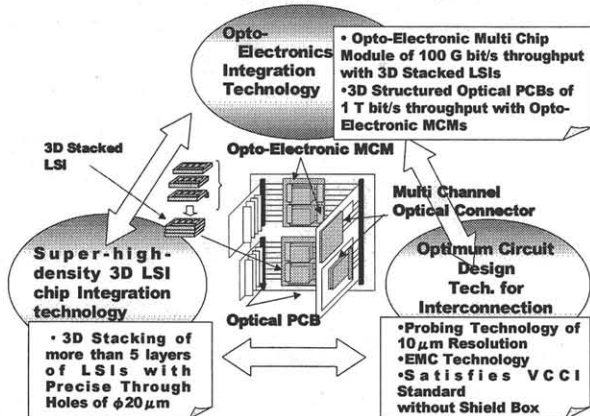


Fig. I Ultra High-Density E-SI project target

3. Current situation of the E-SI project

High density 3D stacked Integration

- Through Via :Research and trial of technology candidates showed the possibilities for through hole electrode formation.
- Chip Thinning:Grinding damage characterization and dry etching test showed damage-free possibilities.
- Chip Stacking:High accuracy bonding for 20 μ m-pitch, comparison of bonding method (metallurgical, non-metallurgical), 3~5 μ m gap encapsulation were tested.

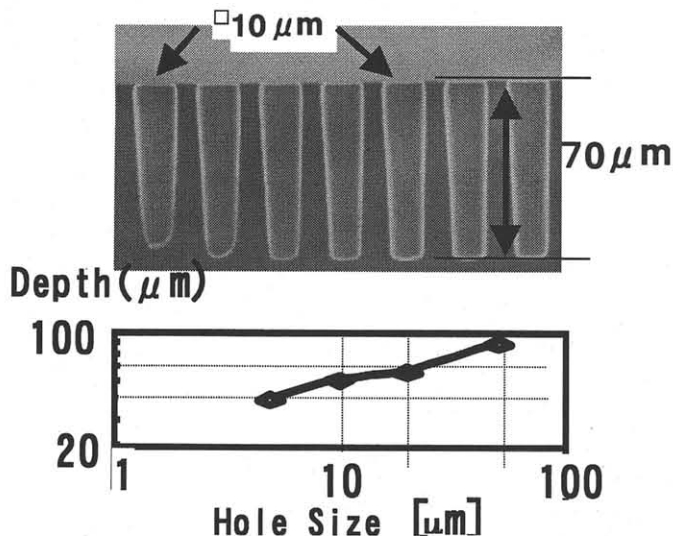


Fig. II Through Hole Formation by RIE

- Inspection & Test:CSAM and X-ray inspection was tested
- 40 μ m-pitch probing with Si-whisker was tested.

-Design:Thermal analysis revealed bump / encapsulation / substrate effects for heat dissipation. Structural analysis indicated small stress value but specific concentration in bump areas.

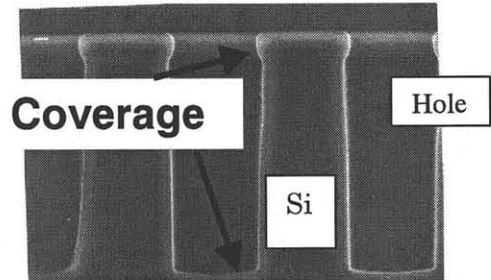


Fig.III Hole :10 μ m Sq. 25 Depth

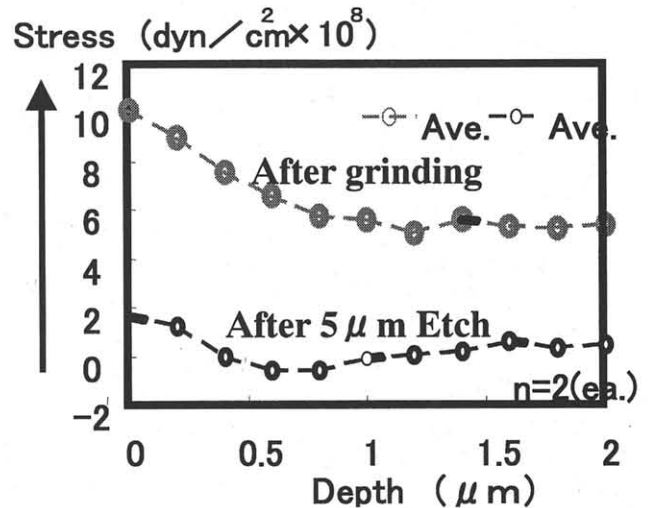


Fig. IV Stress reduction by Dry Etching

- Chip Stacking:High accuracy bonding for 20 μ m-pitch, comparison of bonding method(metallurgical, non-metallurgical), 3~5 μ m gap encapsulation were tested.

Stacking and Testing

-Flip-chip Bonding:

HAB: Micro-bump joint was achieved in 20mm pitch.
UFB, CBB: Fundamental metallurgical bondability was confirmed in 100mm pitch

-Encapsulation:

No Metallurgical: Anisotropic interconnections are hard to apply to 20mm pitch, and NCP is selected as one of the main encapsulation process.

Underfill: Low viscosity resin with no filler realized the encapsulation of the narrow gap between the die and the interposer in 20mm pitch.

-Structure Design:

Thermal: TH electrodes were not so effective compared with the thermal bumps, while the interposer thermal conductivity was the dominant factor.

Electrical: TH electrodes are excellent for high frequency module, although TH dielectric thickness effects capacitance.

Structural: In case of the thin device, the die stress is concentrated above bump.

At any other point, no distinct stress was observed especially for Si Interposer.

-Probing & Inspections:

Probing: Silicone whisker probe was selected, and the required overdrive was confirmed from the stand point of the contact resistance to the gold plating.

Internal Inspections: IR, SAM, and X-ray was evaluated detecting the defects on the bump and the underfill resin in 20mm pitch, which were necessary to be optimized.

Opto-Electronic Packaging Technology

Large OE-MCM board:

- Fundamental research is the main activity for the optical parts, materials, sub-assembly and clarify the R&D items by 3D optical Packaging trial model as this project target.
- Fluorinated polyamide multi-channel optical waveguides with low-loss down to 0.3 dB/cm
- Film-lamination method for economic and simplified fabrication for MCM
- Photo-bleaching technology for further cost-reduced and simplified manufacturing of MCM
- High-precision 40 channel optical alignment-free assembly using multi-chip batch self-alignment
- Right-angled coupling between Optical devices and waveguides using Si "Pyramidal mirrors"

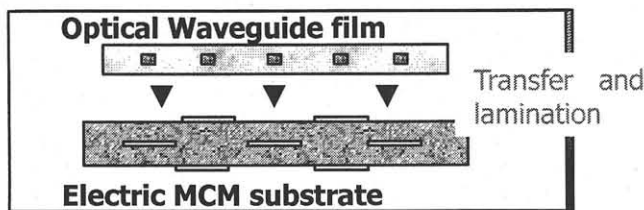


Fig. V -Film-lamination method for economic MCM

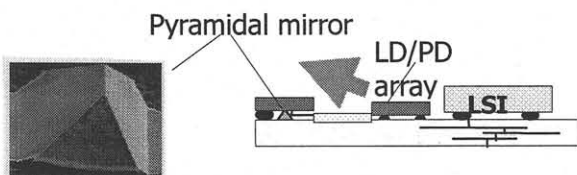


Fig. V I Optical devices & waveguides with "Pyramidal mirrors"

Thermal Management and Active interposer technology:

-High-speed optical complementary interconnection has the feasibility target as 100mW at 1Gbit/s with the Power save of $< 1/5$.

-Basic Concept of Active Interposer:

Mounting 3D-LSI, High Speed (~ 10 Gbit/s) interconnection and Optical and Electrical interconnection are the feature.

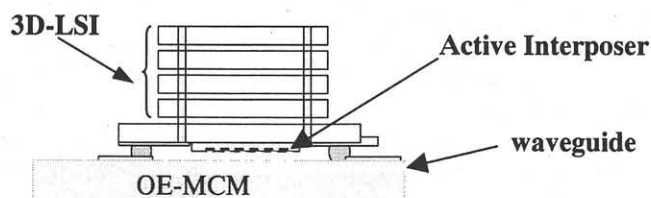


Fig.VII Basic Concept of Active Interposer

Large size and low loss OE-Board : (Size: ~ 600 mm , Loss: < 0.05 dB/cm, Throughput: ~ 500 Gbit/s)

-Interconnect with Opto Connectors, and Opto Devices by two way of optical fiber and polymer waveguide.

-Bending waveguide connector and Crank optical path connector has been also investigated.

-Bookshelf structure optical Bus for Tbits throughput and Skew generation mechanism and dominant factors have been studied.

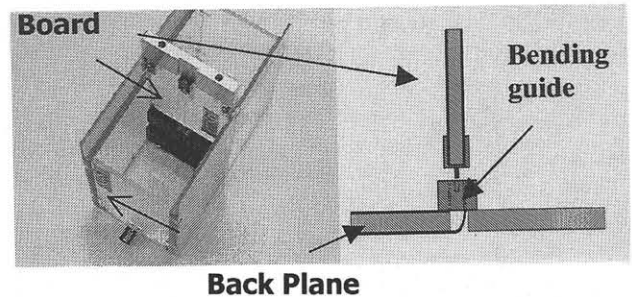


Fig. IX Board-board bending guide connector

Optimum circuit design technology

EMI/EMC matter:

Fundamental technology development has been investigated for solving EMC problems of 3D-LSI chip and Opto-electronic packaging

-Development of EMI probing technology with 10μ m space resolution and high-frequency response.

-Development of EMI reduction technology to satisfy VCCI standard class B without shield box..

-LSI design has been studied for programmable noise generation by CMOS gate array of 0.35μ m process with separated power supply system of core from that of I/O and noise generating circuits by core and I/O circuits.

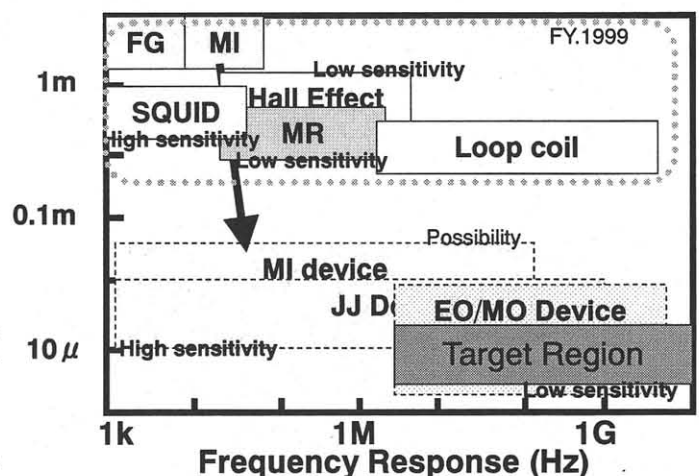


Fig.X Performance mapping of probes

4. Conclusion

-Though this E-SI project research has started only 1 year ago, there found a lot of new possibility in the 3D stacked LSI chip technology, opto-electronics device packaging and interconnecting technology and the optimum circuit design and analyzing EMI/EMC technology for the new seamless information network society.

This activity has been expected to a huge contribution to creating a big new value added market and new mobile wearable electronics and optics combined system in near future. As This project will have the middle range check and evaluation by the NEDO in 1.5 year, the researcher will make their all efforts for installing the fundamental technology progress in this E-SI field.

Acknowledgments

This paper includes all the researchers activity of Electronic System Integration Technology Research Dept. of ASET. I would like to expression my big Thanks for their efforts and their leader Mr. Osamu Ibaragi, Mr. Kenichi Takahashi, Mr. Shigeki Hoshino and Mr. Masakazu Ishino. I could refer their Annual Report and use their data as the represent of this paper making. All E-SI researcher have been got the good suggestion from Mr. Takaaki .Ohsaki (NTT-AT Co. , the NEDO project leader) , his contribution to this new installation of E-SI have been quite large with NEDO people. We deeply [appreciated to these persons and related people.

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