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GHz Signal Propagation through Transmission Line on ULSI Chip

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1. Introduction

In GHz operating ULSI, the global interconnect such as bus line and clock distribution line across *cm*-size chip should be treated as transmission line instead of lumped RC circuit, because the signal wavelength is no longer neglected against the chip size. The importance of inductance components has been pointed out and the clock distribution using transmission line has been reported[1]. For signal transmission through the transmission line, impedance matching among driver, line, and receiver is substantial. However, so far, circuit configuration and transmission line structure on a Si ULSI chip have not been clarified.

In this paper, we discuss the signal propagation through the lossy transmission line with the driver/receivers of Si CMOS inverters.

2. Driver/Interconnect/Receiver Configuration

When the CMOS inverter is used as receiver circuits for simple circuit configuration, the end point of the transmission line has to be treated as open terminal because of the high input impedance of CMOS inverter. This means that one should suffer from the reflection of signal at the receiver input. So that, although the transmission line is used, the circuit operation mode is the conventional charge/discharge type.

Figure 1 shows the equivalent circuit when the CMOS inverter is used as receiver. Table I lists the parameters of the transmission line used in this work. Due to the resistance component, the wire becomes a lossy transmission line. As shown in Fig. 2, ***when the output impedance of the driver R_{out} is matched to the characteristic impedance of the line***, the voltage at the load capacitances rises steeply when the signal reaches at the load capacitance. It is noted that, although the voltage at the end port of the line rises to signal swing (E) after the propagation delay (τ_{line}) of the line, the voltage at each point on the line reaches to the input signal swing (E) after the round trip duration, which is equal to twice of the propagation delay of the line ($2\times\tau_{line}$).

3. Drivability of Receivers on Transmission Line

Figures 3(a) and (b) show the lossy transmission line with driver/receivers CMOS inverter. The 4-receivers of CMOS inverters are connected to the transmission line. Figure 4 is simulated output signals of each receiver when the gate width ratio of the driver $(W_n/W_p)^D$ is changed. In the simulation, transmission line is expressed distributed RLC circuits. Since the output impedance of the CMOS inverter is approximately estimated to be $R_{out}=1/G_m=V_{DD}/I_D$ at $V_G=V_{DD}$ (Table II), waveforms are changed depending on the driver gate width. When $(W_n/W_p)^D$ is 60μm/120μm, the output impedance of CMOS driver is approximately matched to the line. The delaytime $\tau_{R\text{-}90\%}$ and $\tau_{F\text{-}90\%}$ are 320ps and 305ps. The intrinsic gate delaytime $\tau_{R\text{-}90\%}{}^g$ and $\tau_{F\text{-}90\%}{}^g$ are 107ps and 91ps, and the round trip time of the 2cm wire is $2\times\tau_{line}=2\times133$ps, the delaytime $\tau_{90\%}$ is less than $(\tau^g+2\times\tau_{line})$.

As shown in Fig. 4(b), it has been found that the delaytime deviation $\Delta\tau_R$ and $\Delta\tau_F$ is less than 10ps. This can be explained as follows. Figure 5 shows the input signals of each receiver, v_i^n, (n=1, 2, 3, and 4). Although v_i^n rises at the different timing depending on the position of receivers, the timing when the signal crosses the inverter threshold of $(1/2)V_{DD}$ almost at the same because of the loss of the transmission line.

Figure 6 summarizes the delaytime and delaytime deviation as a function of gate width of nMOS. The delaytime deviation has minimum when the output impedance is matched to the characteristics impedance of the line. This means that, although the circuit of Fig. 3(a) has open terminal, the delaytime is averaged by the effect of resistance loss of the line.

Using this averaging effect of lossy transmission line, the bus line drive of Fig. 3(b) is available. In this case, the driver is connected at the middle of the line. When $(W_n/W_p)^D$=60μm/120μm, $\tau_{R\text{-}90\%}$=314ps and $\tau_{F\text{-}90\%}$=281ps, and delaytime deviation is less than 5ps.

4. Summary

We discuss the CMOS-inverter driver/receiver and transmission line configuration for GHz signal propagation. It is found that, for the charge/discharge type interconnect, when the driver output impedance is matched to the characteristic impedance, the receivers connected to the lossy transmission line can be driven without delaytime deviation. Furthermore, this configuration can be employed for the GHz bus line where the drivers are connected at the arbitrary position of the line.

References

[1] M. Yamashina and M . Mizuno, 1999 SSDM, pp. 586.

TABLE I. Parameters of transmission line

Characteristic impedance: (Dielectric constant: ε_r=4.0)
$Z_o=(L_o/C_o)^{1/2}=50$ [Ω] $L_o=0.333$μH/m, $C_o=0.133$nF/m
Velocity(v_p) $=1/(LC)^{1/2}=1.5\times10^8$ m/s, 66.7psec/cm
Resistance: R = 3kΩ/m (30Ω/cm)
This corresponds to 5μm-wide/2μm-thick Al wire.

TABLE II. Performance of AMS* 0.3μm CMOS

nMOS	I_D = 5.3mA (@V_G=V_D=3.3V, W_n** = 10μm)
pMOS	I_D = 2.4mA (@V_G=V_D=3.3V, W_p** = 10μm)

*) AMS: Austria Mikro Systeme International

**) W_n W_p: gate width

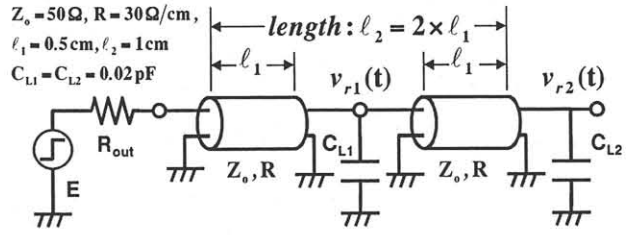


Fig. 1 Transmission line with capacitor loads.

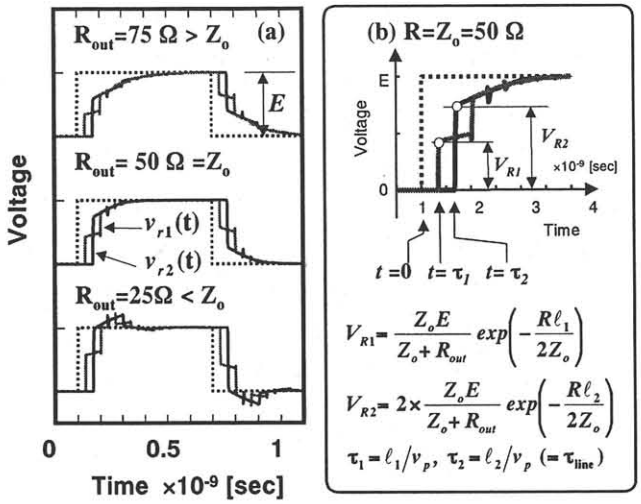
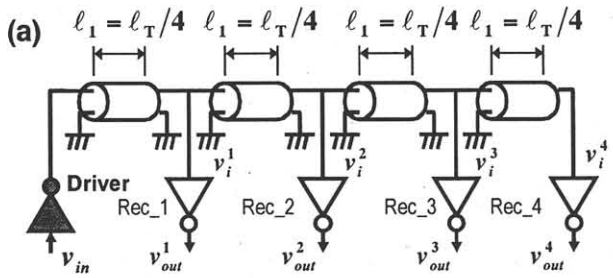
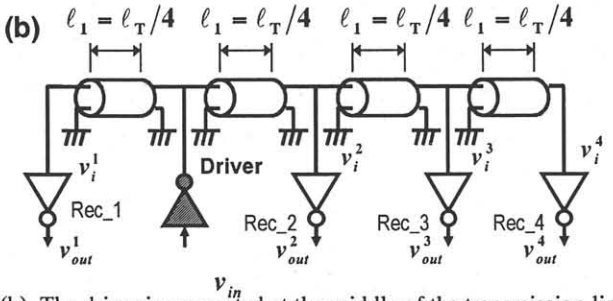


Fig. 2 Voltage signals of Fig. 1.



(a) The driver is connected at the end port of the transmission line.



(b) The driver is connected at the middle of the transmission line.

Fig. 3 Transmission line with 4-receiver circuits. The wire length ℓ_T is 2cm. The driver and receivers are CMOS inverters. The gate width ratio of the receiver is $(Wn/Wp)^R$=1.5μm/3μm.

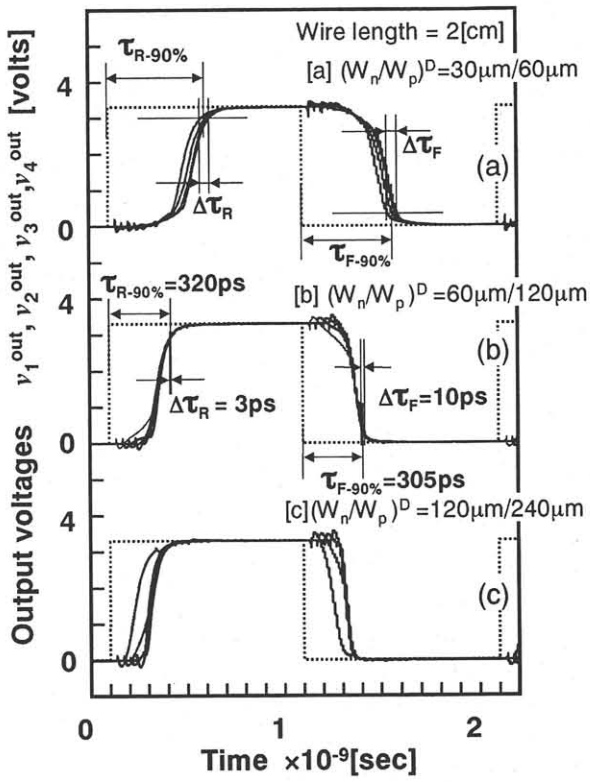


Fig. 4 Output signals of each receiver of Fig. 3(a). $(Wn/Wp)^D$ is the gate width ratio of CMOS driver circuit. $\tau_{90\%}$ without line, *i.e.*, intrinsic gate delay is $\tau_R^{90\%}$=107ps and $\tau_F^{90\%}$=91ps.

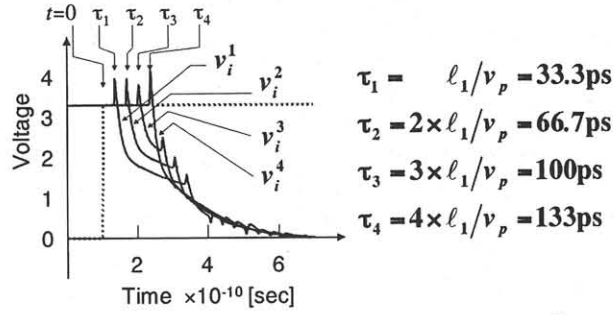


Fig. 5 Input signals of each receiver of Fig. 3(a). $(Wn/Wp)^D$ = 60μm/120μm.

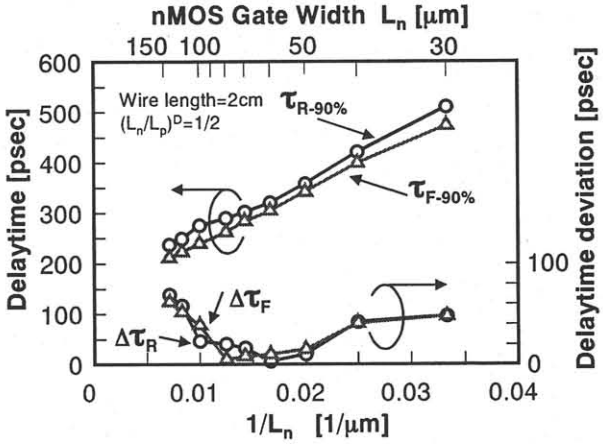


Fig. 6 Delaytime and delaytime deviation as a function of nMOS gate width. Delay time $\tau_{R\text{-}90\%}$ and $\tau_{F\text{-}90\%}$ are defined as average delay time of 4-receivers.