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Progress of Three-Dimensional Integration Technology

Mitsumasa Koyanagi

Department of Machine Intelligence and Systems Engineering, Graduate School of Engineering, Tohoku University
01 Aza-Aoba, Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone: +81-22-217-6906 Fax: +81-22-217-6907 e-mail: koyanagi@sd.mech.tohoku.ac.jp

1. Introduction

An internal clock frequency of LSI chip rapidly increases with scaling-down the device size. However, the external clock frequency less rapidly increases since it is very difficult to quickly drive the package pins and the external wirings on the board. To increase the external clock frequency and the data transfer speed between LSI chips, the pin capacitances and the wiring length have to be reduced. We can reduce the pin capacitances and the wiring length by using three-dimensional (3D) integration technology. The 3D integration technology is also useful to increase the wiring connectivity within a chip. In a near future, it will become difficult to catch up with the increasing demand to a higher wiring connectivity only by increasing the number of the metal layer. Several chip layers can be vertically stacked and a huge number of interconnections can be formed in the vertical direction by using 3D integration technology and hence we can dramatically increase the wiring connectivity and reduce the number of long wiring. In this paper, we discuss about the 3D integration technology to achieve new System-on-Chip (SoC) and System-on-Package (SoP).

2. Three-Dimensional Integration and Packaging

The 3D integration technology is classified into three categories of package level, chip level and wafer level. The 3D integration in package level can be called 3D packaging. The 3D integration in chip level and wafer level can be also considered to be 3D packaging although it is called 3D LSI. Recently, LSI technology tends to merge with the packaging technology. A Chip Size Package (CSP) is a typical example of merging LSI technology with packaging technology. Therefore, the 3D integration in chip level and wafer level can be also called a chip level 3D-CSP and wafer level 3D-CSP, respectively.

3. Wafer Level Three-Dimensional Integration

A typical example of wafer level 3D integration and wafer level 3D-CSP is shown in Fig.1. The fabrication sequence is illustrated in Fig.2. The device wafer with the buried interconnections are glued to a quartz glass and then thinned from the back side using the mechanical grinding and CMP. The micro bumps are formed on the bottom of the buried interconnections at the back side.

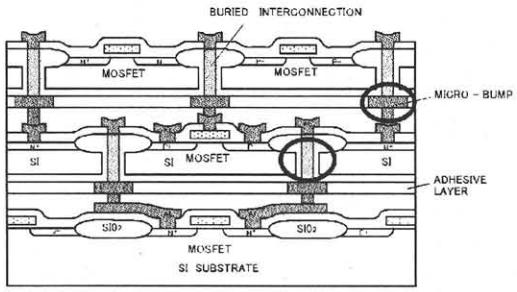

Fig.1 Stacked structure by wafer level 3D integration.

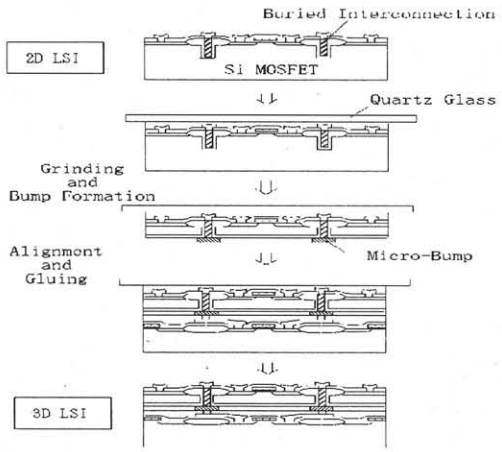

Fig.2 Fabrication sequence in wafer level 3D integration.

This thinned device wafer is glued to the another device wafer after a careful wafer alignment. By repeating this sequence, the 3D stacked wafer can be obtained. To achieve such 3D chip, we have developed five key technologies such as formation of buried interconnection, micro-bumps, wafer thinning, wafer alignment and wafer bonding. It is required to form the deep Si trenches in order to form the buried interconnections which act as vertical interconnection. The 2 μm Si trench with depth of around 60 μm was formed using Inductively Coupled Plasma (ICP) etching. Then, the Si trench was oxidized and filled with n+ poly-Si (0.4mΩ-cm) by LPCVD. The wafer is thinned to around 30 μm from the back side surface using grinding and CMP techniques after bonded to the quartz glass which acts as a mechanical supporting material. In-Au micro bumps are formed on the back surface using the lift-off technique. Then, the thinned wafer are aligned to the bottom device wafer with the

alignment tolerance $\pm 1\ \mu$m using a newly developed 3D wafer aligner. This wafer aligner can also provide an uniform force raising the temperature to guarantee a firm contact between the upper and lower micro bumps. In-Au micro-bumps and epoxy adhesive layer are used to bond two wafers. The liquid epoxy adhesive is injected into the gap between two wafers in a vacuum chamber after the temporary bonding using the micro bumps.

4. Test Chip for New Three-Dimensional System

We have proposed various kinds of new system-on-silicon LSIs or system LSIs based on our new 3D integration technology. A real time micro-vision system LSI as shown in Fig.3, a merged memory and logic LSI as shown in Fig.4, a real shared memory for parallel processor system and 3D artificial retina chip are typical examples of these new system LSIs. We have designed and fabricated a test chip for these new 3D system LSIs. Fig.5 shows the SEM cross-section of 3D LSI test chip fabricated using 3D integration technology. It is clearly observed that three wafer layers are well aligned and uniformly bonded through the microbumps and insulating epoxy adhesive. The electrical characteristics of this 3D LSI test chip were evaluated and then we obtained the values of around 9 Ω for the resistance of buried interconnection and around 10 m Ω for the contact resistance of microbumps. In addition, excellent transistor characteristics were obtained in the 3D test chip even after wafer stacking.

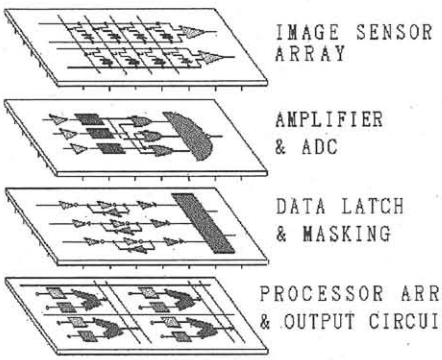

Fig.3 3D system LSI for real time image processing.

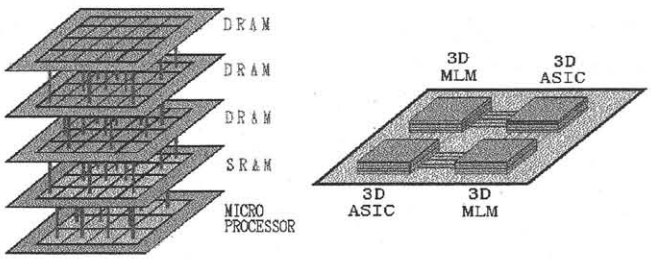

Fig.4 Merged memory and logic LSI (3D computer chip).

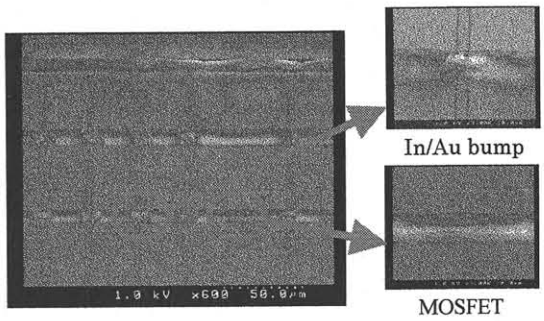

Fig. 5 SEM cross-section of 3D LSI chip with 3 layers.

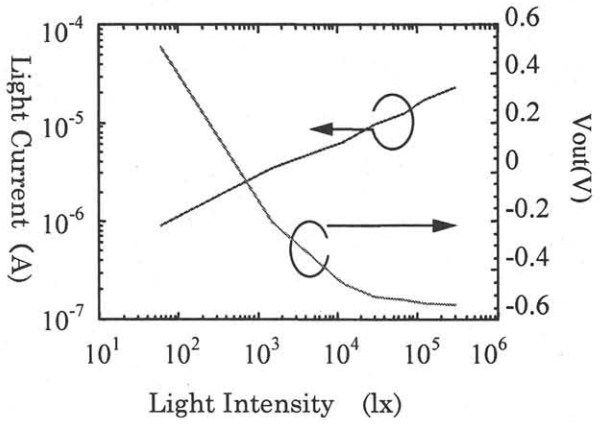

Fig.6 Output characteristics of stacked 3D image sensor chip as a function of input light intensity.

Leakage current was very low (below 10^{-9} A) even for V_d and V_g of 3.0 V. The electrical characteristics of a stacked 3D image sensor test chip were evaluated through the buried interconnections and microbumps. Fig.6 shows the photodiode current and basic characteristics of stacked 3D image sensor test chip where the optical signal is well detected.

5. Conclusion

It was shown that new system-on-chips and system LSIs can be realized by using three-dimensional (3D) integration technology and the 3D integration technology facilitates LSI technology to merge with packaging technology. It was demonstrated that 3D image sensor test chip fabricated using a new wafer level 3D integration technology shows excellent characteristics.

Acknowledgement

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References

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