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Deep Trench Etching in SOI Wafer for Three-Dimensional LSIs

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1. Introduction

Recently, three-dimensional (3D) integration technology has attracted much attention since it offers the possibility of solving the serious interconnection problems in future LSIs. To realize high-performance and highly parallel processing LSIs, we have developed a new 3D integration technology using a novel wafer level bonding technique. We have fabricated 3D stacked image sensor chip and evaluated its electrical characteristics using bulk Si substrate [1-2]. However, to achieve high speed and low power operation SOI devices are preferable. Then, the new integration technology for SOI substrate becomes demand. In this work, we report the deep trench etching characteristics in SOI wafer using high-density inductively coupled plasma (ICP) etching.

2. New 3D LSI technology using bonded SOI

A cross-sectional view of our 3D LSI is shown in Fig. 1 where several chip layers are vertically stacked and more than 10^5 interconnections per chip are formed in the vertical direction. To realize these 3D LSI, we used bonded and etch-back SOI (BESOI) wafer with 0.5 μm thick buried oxide layer as a starting wafer. The fabrication sequence of BESOI wafer is shown in Fig. 2. First, the base wafer is brought into contact with device wafer with 0.5 μm thick oxide applying the external pressure at room temperature. These wafer sandwiches are annealed for two hours at 1150°C in a N_2 ambient. The device wafer in SOI structure is then thinned by mechanical grinding and CMP method to around 50 μm. Figures 3(a) and 3(b) show the SEM cross-sectional view of as-bonded and after thinned BESOI wafers, respectively. It is necessary to form deep Si trenches for the buried interconnections, which acts as vertical interconnections in the thinned device wafer. The Si trench was formed by ICP etching, which is satisfying the requirements: high etch rate, good selectivity to masking material, and anisotropy. This work was performed using a Multiplex ICP etcher. The etch rate has a strong dependence on the trench width, we used a uniform pattern width of trench with 2 μm square.

3. Results and discussion

(1) Etching characterization of Si trench

Electrode power dependent etch: Anisotropy has a strong dependence on electrode power, which increases the ion directionality and hence etching anisotropy. However, the greater electrode power decreases the selectivity to the photoresist which is used as a masking material. Thereby, it is necessary to optimize the electrode power to achieve high anisotropy and good selectivity. When the electrode power is increased, the trenches become negatively tapered, as shown in Fig. 4, where the electrode power increased, the bottom of trench is more positively charged and then the sidewall etching occurred at the bottom of trench.

Resist dependent etch: In dry etching process, the etching characteristics are dependent on thickness of the mask materials. Increasing the thickness of photoresist, the etch rate decreased, as shown in Fig. 5, because the ion flux is deflected due to charge-up by photoresist. Increasing thickness of resist, the incident ions are more deflected, then the amounts of positive ions which contribute to etching are decreased. Furthermore, the depth of trench is varied with the position in adjacent trenches in thicker resist although the pattern size is identical. The depth of trench at the side position is shorter than that of the center position in 5 μm thickness, however, the etch rate is identical irrespective to the pattern positions when the resist thickness is less than 3 μm as shown in Fig. 6.

Cycle duration dependent etch: Cycle duration starts with an etching cycle flowing SF_6 only, and then switches to passivating cycle using C_4F_8 only. When the passivation time is shorter than that of etching, the sidewall etching occurred at the bottom of trench due to lacks of passivation. Increasing passivation time, the passivation of sidewall increased, then the sidewall shape becomes anisotropy. However, the greater passivation decreased the etch rate, as shown in Fig 7.

(2) Etching characteristics for buried oxide in SOI wafer

During the Si trench etching in SOI wafer, the buried oxide layer emerged when the Si trench is completed. However, the buried oxide layer were not etched by the etching conditions for Si trench, and significant sidewall etching (notch) of Si occurred at the surface of oxide due to accumulated positive ions, as shown in Fig. 8. In order to resolve these problems, we developed multi-step etching process which optimized the etching conditions and employed the appropriate feed gas. When approaching to the buried oxide layer, we change the etching parameters to increase passivation effect where the small amounts of C_4F_8 gas flow with SF_6 gas as shown in Fig. 8. After deep Si trench etching, the buried oxide should be etched for the buried interconnection. We investigated the influence of etching parameters such as etching conditions and plasma sources on the etching of buried oxide. We optimized etching conditions for buried oxide using CF_4-H_2 system. Figures 9 shows the SEM cross section of Si trench which was etched using multi-step etching processes. It is clear in the figure that the deep Si trench and buried oxide layer are well etched and not appeared notch problem.

4. Conclusion

In order to find the optimal deep trench etching condition in SOI wafer for 3D LSIs, we investigated the dependence of etching characteristics on etching parameters using ICP etching. We developed a new multi-step etching process for solving the notch problem and to form a deep trench through Si substrate and buried oxide in SOI wafer.

Reference

1. M. Koyanagi et al., IEEE MICRO 18(4), p17 (1998)
2. H. Kurino et al., Tech. Dig. IEDM, p879 (1999)

Acknowledgement

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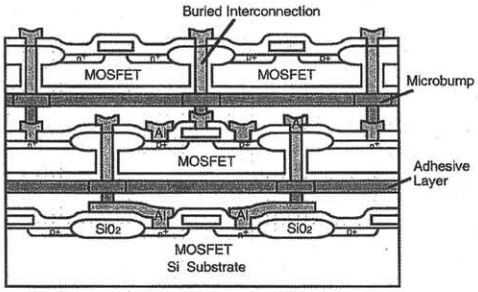


Fig. 1. Cross section view of 3D LSI

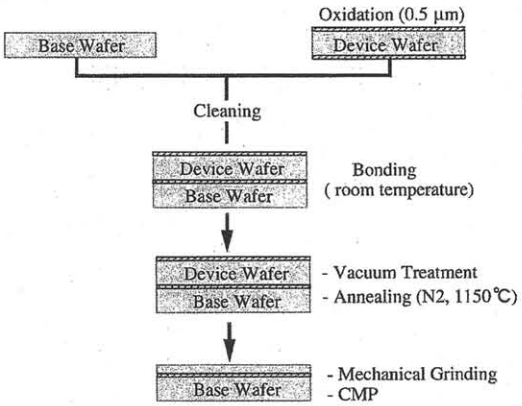
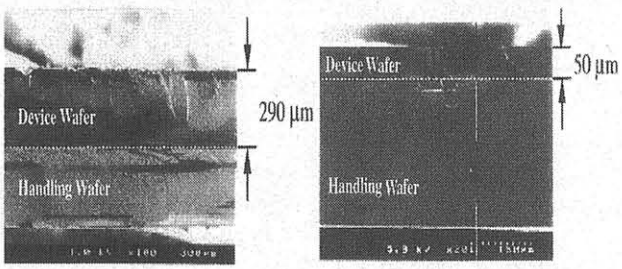
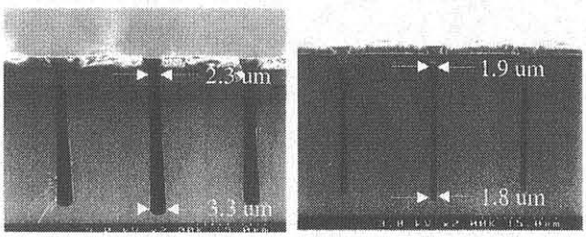


Fig. 2. Fabrication sequence of BESOI wafer



(a) (b)

Fig. 3. SEM cross section of as-bonded and after thinned



(a) 30W (b) 10W

Fig. 4. SEM cross section of trench with electrode power

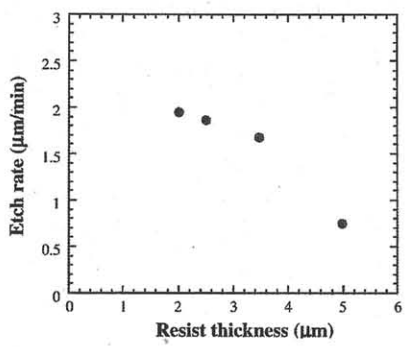
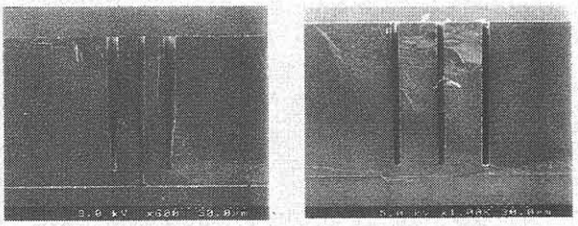
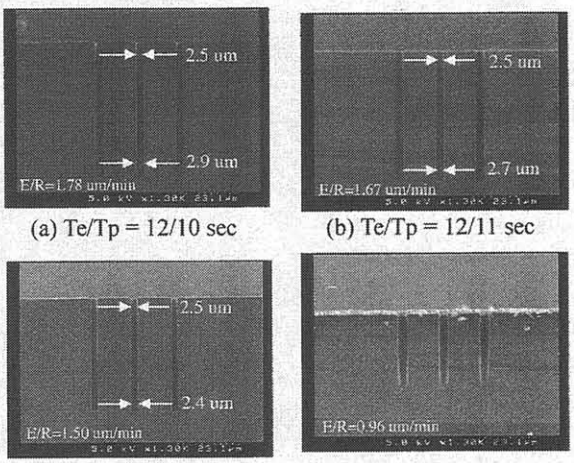


Fig. 5. Etch rate dependence with the thickness of resist



(a) Thickness : 5.0 um (b) Thickness : 3.0 um

Fig. 6. SEM cross section of trench with the resist thickness



(a) Te/Tp = 12/10 sec (b) Te/Tp = 12/11 sec

(c) Te/Tp = 12/12 sec (d) Te/Tp = 12/13 sec

Fig. 7. SEM cross section of trench with cycle duration time

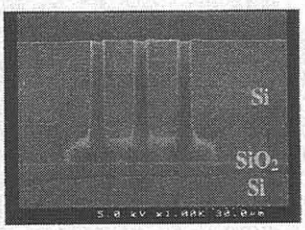
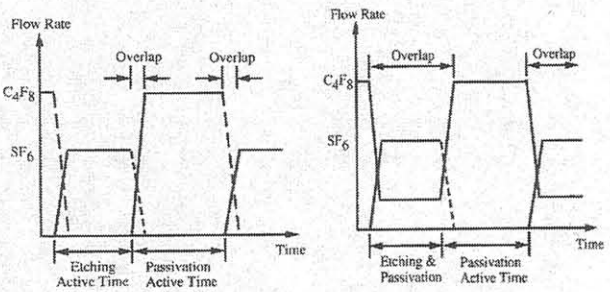


Fig. 8. Notch phenomenon in SOI structure due to build-up charges



(a) 1st step for upper Si (b) 2nd step for lower Si

Fig. 9. Schematic presentation of step etching process

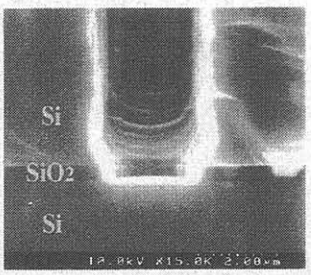


Fig. 10. SEM cross section of trench etching in SOI structure without notch problem using multi-step etching process