Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 426-427

A-9-3

Fine Pitch CSP Technology Using Au Ball Bumps as External Terminals

Shinsuke Nakajyo, Masanori Onodera, Masamitsu Ikumo and Toshimi Kawahara
Advanced Packaging Tech. R&D Dept. LSI Packaging Div., Fujitsu Ltd.
4-1-1, Kamikodanaka, Nakahara-Ku, Kawasaki 211-8588, Japan
Phone : +81-44-754-2503 Fax : +81-44-754-2334 e-mail : nakajo@pkga.ed.fujitsu.co.jp

1. Introduction

In the development of CSPs, the bump pitches have already been reduced to 0.5mm or 0.4mm. In the first half of year 2000, the pitch is estimated to reduce to 0.3mm. The CSP development currently in vogue is an area array type CSP typified by fine pitch BGA(Ball Grid Array). This type of CSP can cover a wide range of numbers of I/Os. Unlike peripheral placement packages such as the existing 0.3mm pitch QFP(Quad Flat Package), however, it is necessary to draw out the wires to draw out the wires on the substrate immediately under the package after mounting the chip. Therefore, as the bump pitch reduces, it may be necessary to use a multi-layer substrate, resulting in the increase in cost and limiting the application of the package.

In addition, soldering is widely used as a bump material in the present CSP but elimination of lead is an issue we cannot avoid even if soldering is continued to be used as a material for the bump of the fine pitch CSP. Before CSPs are put into practice use and widely used, we will have many technical hurdles to get over.

Therefore, Au ball bumps, which has been used for bare chip assemblies, were applied as external terminals and a trial CSP was produced where these bumps were arranged just inside edges of the CSP. This paper reports the new structure and assembly technology of this CSP.

2. Package structure

Fig.1 and Fig.2 show the outer shape photograph of the trial model of a CSP and schematic drawing the cross-sectional structure, respectively. The CSP does not contain an interposer in it and consists of very small amount of materials. At the bottom of the CSP, the gold ball bumps are arranged in 0.2mm pitches and are connected to the wires exposed at the bottom. Because of this structure, the bump pitch can be reduced to the level of the wire bonding pitch technically and any pitch can be selected depending on the method of wire bonding. Though the body size is larger than the chip due to the existence of wires, the expansion of the body size can be minimized even for a chip having many I/O pins by narrowing the pitch.

The substrate used in the process has a simple structure of a copper alloy plane plated with silver. Therefore, It is possible to package various types of LSI chip on only one substrate type.

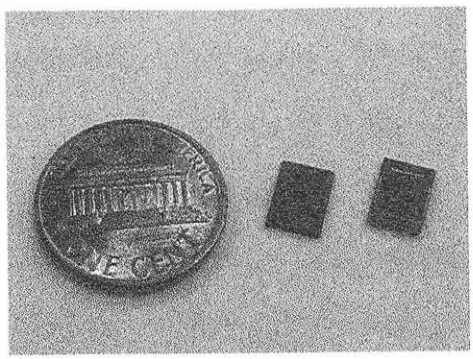

Fig. 1 Photograph of the Outer shape of a trail CSP.

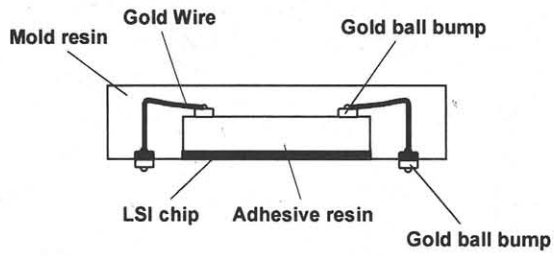

Fig. 2 Schematic drawing of the cross sectional structure of a CSP.

3. Assembly process

Fig.3 shows the assembly flow chart. A leadframe is temporarily used as an interposer in the process. In the wire bonding process, which is after chip mounting process, wires after ball bonding on silver plating were lifted and they were stitch bonded on the gold ball bumps formed on the electrode pad the LSI chip in advance.

In the leadframe-removing process, the leadframe was dissolved by etching with the anmonia etchant solution for copper circuit formation for printed wiring boards. Fig.4(a) shows the SEM photograph of the surface exposed after removing the leadframe. The manufacture process utilizing dissolving leadframe has been put to practical use for a CSP[1], we took notice of the dissolution ability not only for Cu alloy but for Ag plate. The dissolution rate of Ag plate is lower than that of Cu alloy, but the whole etching time is sufficiently allowable for packaging process.

In the bump-forming process, the gold wires exposed on the bottom of the package are connected directly. Fig.4(b) shows the SEM photograph of the gold ball bumps formed on the bottom of the package. To keep the high yield in this process, it is necessary to optimize the exposed wire diameters and gold ball bump dimensions while considering the bonding misalignment of both the wires and gold ball bumps. In addition, since residual Au-Ag compounds are formed on the exposed wire surfaces, the influence on bump forming needs to be confirmed. Therefore, we performed the shear test for interface between Au ball bumps and exposed wires after temperature cycling (-55/125 ℃). Fig.5 shows the dependence of the bonding conditions (bonding loads). Since the shear strength did not decrease even after 1000cyc., the reliability is sufficiently allowable.

4. Conclusion

This paper reported the CSP with Au ball bump terminals and its assembly technology. Au ball bumps are applied not only to this trial CSP structure but also to various kinds of LSI packages and have the potential to become an alternative of the fine pitch technology below 0.3mm pitches in the future.

Reference

[1]M.Onodera et al., "Development of BCC(Bump Chip Carrier)" 3rd Symposium on Microjoining and Assembly Technology in Electronics, Yokohama, Japan, Feb.6-7, pp.33-38, 1997

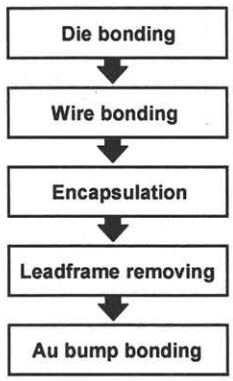

Fig. 3 Assembly process flow.

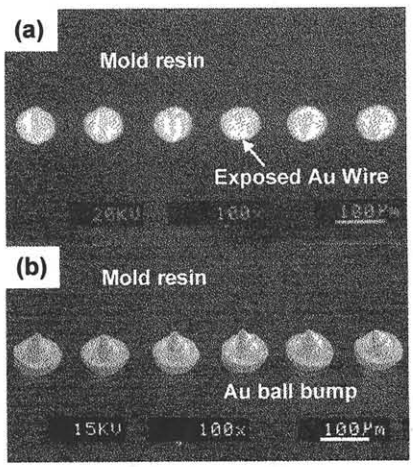

Fig. 4 SEM photographs of (a)exposed gold wire tips after etching dissolution and (b)Au ball bumps on the exposed gold wire tips.

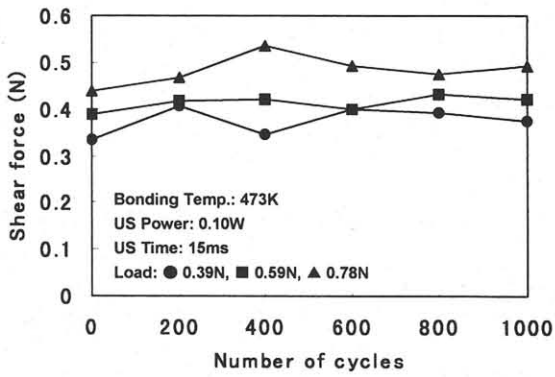

Fig. 5 Dependence of the bonding condition.