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The Impact for Gate Oxide Scaling (32Å-12Å) and Power Supply for Sub-0.1 μm CMOSFETs

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1. Introduction

As MOSFETs are scaled down to 0.1μm and below, ultra thin gate oxides are needed to keep high drive performance and to control short channel effect (SCE). Unfortunately, gate oxide scaling gives rise to many undesirable effects. In this work, we investigate the tradeoffs and optimization of gate oxide thickness as well as power supply voltage for a high performance sub-0.1μm gate length CMOSFET. The device design constraints in terms of gate oxide scaling was also evaluated

2. Experiment

After shallow trench isolation (STI) followed by MeV well implantation, dual gate CMOSFETs were fabricated with various physical gate oxide thickness ($T_{ox\_phys.}$ = 32Å – 12Å) grown by rapid thermal oxidation in N_2O ambient. 2000 Å poly-Si gate electrode was formed with rapid thermal deposition with post phosphorus doping (for n^+ poly-Si gate) followed by post thermal annealing. Source/drain extension implantation were employed prior to SiN spacer formation. Deep n^+ and p^+ junctions were formed by arsenic and boron implantation in respectively. After $CoSi_2$ salicidation, backend metallization was fulfilled. In this work, MOSFET structures with poly-Si finger overlapped source/drain area (40 x 320 μm²) were used to get reasonable C-V and I-V characteristic of device.

3. Results and Discussion

As gate oxide thickness is reduced, gate oxide leakage was also increased. Figure 1 illustrates the I-V characteristics for MOS capacitors, anomalous leakage current (> 1mA/cm² at 1V accumulation condition) was happened at gate oxide thickness less than 16Å. Figure 2 shows the fitting curve of gate oxide leakage versus $T_{ox\_phys.}$ with various V_{CC}. It is apparent that the $T_{ox\_phys.}$ can be predicted by gate oxide leakage current [1]. Simple equations that evaluate $T_{ox\_phys.}$ from these gate currents are $T_{ox\_phys.}(Å) = 15.3(Å) - 1.005*\ln(J_G(A/cm^2))$ for V_{CC} =1.8V and $T_{ox\_phys.}(Å) = 9.4(Å) - 0.972*\ln(J_G(A/cm^2))$ for V_{CC} =1V. However, electrical gate oxide thickness (T_{oxe}) is more reasonable to response the device performance. Capacitance-voltage (C-V) characteristics were also measured (freq. = 100kHz) for oxides representing V_{CC} and $T_{ox\_phys.}$ ranging from 32Å to 12Å, as shown in Fig. 3. As gate oxide thickness is reduced, quantum effect becomes increasingly significant in oxide thickness extraction and device modeling [2]. Due to tilted curve of C-V plot happened at accumulation conditions, it is hard to predict T_{oxe} from C-V curve at accumulation bias. It is more reasonable to measure T_{oxe} from C-V plot at inversion conditions. However, the band bending was still happened at inversion bias as $T_{ox\_phys.}$ less than 18Å due to poly depletion effect [3]. In the meantime, larger gate oxide tunneling leakage happens and resulting in the C-V curve distortion [4]. Figure 4 shows the gate oxide thickness predicted from gate oxide leakage ($T_{ox}\_I_G$) and from C-V curve (T_{oxe}). T_{oxe} is larger about 8-10Å than $T_{ox}\_I_G$ and is similar to the prediction of K. Yang *et. al.* [1] The difference between the T_{oxe} and $T_{ox\_phys.}$ is dependent on poly depletion effect and gate oxide leakage. From these curves, ideal gate oxide material was required with thinner T_{oxe} and thicker $T_{ox\_phys.}$ (low gate leakage). Therefore, it is very hard to get a gate oxide material with T_{oxe} < 25Å and low gate leakage (< 0.1mA/cm²).

For CMOSFET's design, SCE margin of device can be improved with thinner gate oxide, as shown in Fig. 5. The V_T roll-off (L_{eff}=0.22 → 0.11μm) can be improved as $T_{ox\_phys.}$ from 32Å to 18Å (ΔV_{TN}=50mV → 25mV and ΔV_{TP}=100mV → 50mV for n- and p-FETs in respectively), and becomes not apparently as $T_{ox\_phys.}$ < 18Å due to the poly depletion effect was also increased. By the way, the device's subthreshold swing can be also improved with thinner $T_{ox\_phys,}$ and becomes not sensitive to gate oxide scaling as $T_{ox\_phys.}$ < 18Å, as shown in Fig. 6. For low power CMOSFET's design, the driving capability of CMOSFET was limited by off state drain current (I_{off}). The I_{off} which measured at drain terminal is combined by three component, gate leakage (I_{offG}), source current (I_S), and substrate current (I_{SUB}). In our measurement, I_{SUB} < 1pA/μm and not be affected as gate oxide scaling; thus, majority of I_{off} is caused by gate leakage or source barrier lowing. In order to verify the impact of I_{offG} on I_{off}, off state gate leakage (I_{offG}) versus off state drain current (I_{off}) with various $T_{ox\_phys.}$ at V_D = 1.5 V; V_G=V_S=0V was shown in Fig. 7. For short channel (L_G< 1μm) CMOSFETs, the I_{off} is larger than I_{offG} even as $T_{ox\_phys.}$ = 12Å; thus, the off state leakage of MOSFETs was not caused by gate leakage and can be reduced with higher threshold voltage. Fig. 8 shows the n-FET's I_{drive} versus I_{off} curve for various $T_{ox\_phys.}$ with same threshold voltage (V_{TN}=0.4V), it is apparently that the device's SCE margin can be improved with thinner T_{ox_phys} and $I_{D.SAT}$ of 15 μA/μm was increased per 1Å oxide thickness (I_{off} = 1nA/μm at V_{CC} =1.5V). In this work, how CMOSFET speed was affected by gate oxide and supply voltage scaling has been also investigated. Due to the competing effects of oxide thickness scaling resulting in increased $I_{D.SAT}$ as well as load capacitance simultaneously; thus, optimum T_{oxe} for minimum t_{pd} (T_{oxe}^{OPT}) was depends on load capacitance [4]. Due to poly depletion effect, it has been seen that thinner (T_{oxe}^{OPT}) of devices can be reached at lower V_{CC}, as shown in Fig. 9. Thus, higher dielectric constant gate oxide material was necessary to increase process window of (T_{oxe}^{OPT}) for CMOSFET's performance. With this prediction, this technology was also employed on 0.1μm CMOSFET (nitride gate oxide with $T_{ox\_phys.}$=18Å and SiN spacer). Well-behaved subthreshold characteristics of 0.1μm CMOSFET were obtained, as shown in Fig. 10. Good current drive, $I_{D.SAT}$ of 725μA/μm and 310μA/μm for n-FET and p-FET are achieved with I_{off} of 7.5nA/μm and 5.7nA/um at V_{CC} = 1.2V in respectively.

4. Conclusions

In this work, we investigate the tradeoffs and optimization of gate oxide thickness as well as power supply voltage for a high performance sub-0.1μm gate length CMOSFETs.

References

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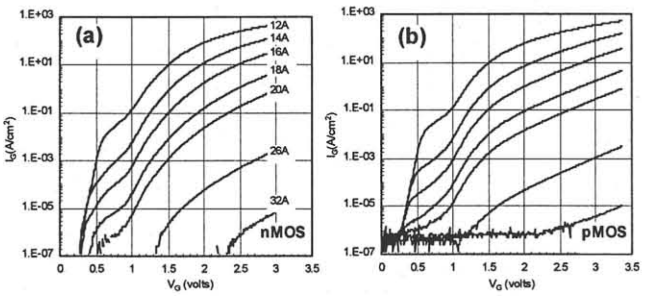

Fig. 1. Measured I_G-V_G characteristics under accumulation conditions of (a) n-FETs and (b) p-FETs with oxides ranging from 32 Å to 12Å.

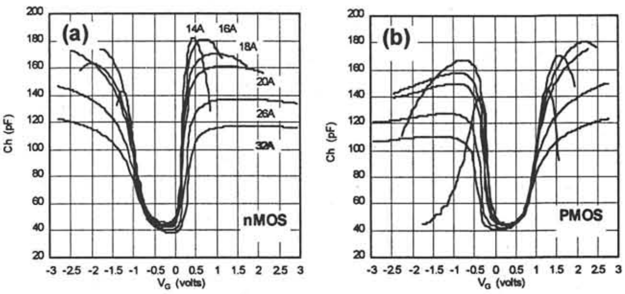

Fig. 3. Comparison of measured gate oxide capacitance versus gate voltage curves for MOS capacitors with (a) n-type and (b) p-type substrates and oxides ranging from 32 Å to 12Å.

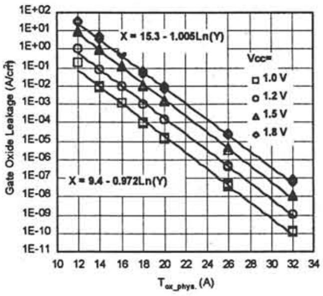

Fig. 2. Comparison of measured gate oxide leakage versus physical gate oxide thickness with various V_{CC}.

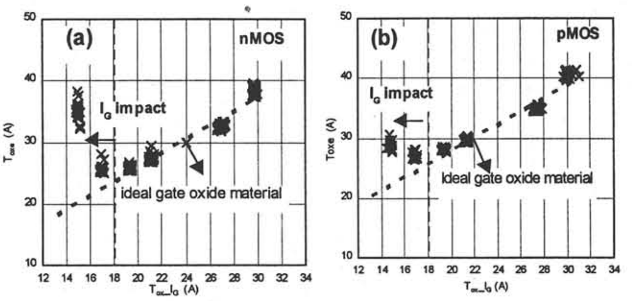

Fig. 4. Comparison of measured gate oxide thickness predicted from gate leakage (T_{ox}_I_G) versus electrical gate oxide thickness predicted from C-V curves (T_{oxe}) for (a) n-FETs and (b) p-FETs

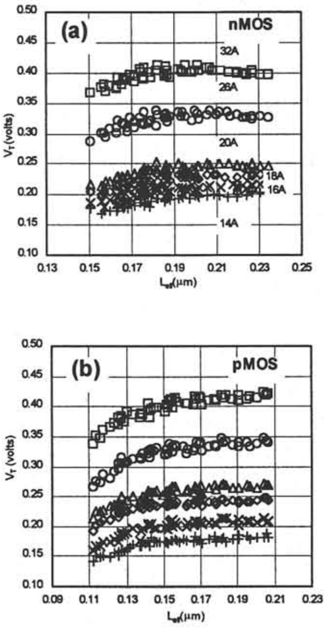

Fig. 5. Comparison of measured threshold voltage versus effective gate length curves for (a) n-FETs and (b) p-FETs with oxides ranging from 32 Å to 14 Å.

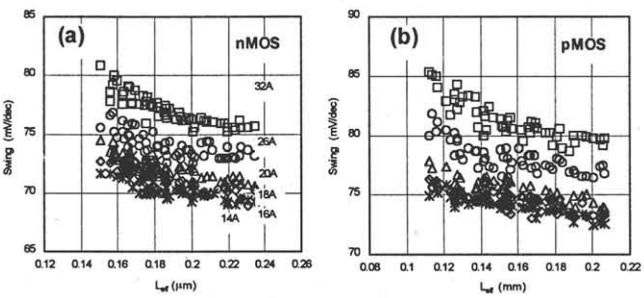

Fig. 6. Comparison of subthreshold swing versus effective gate length for (a) n-FETs and (b) p-FETs with gate oxides ranging from 32 Å to 14 Å.

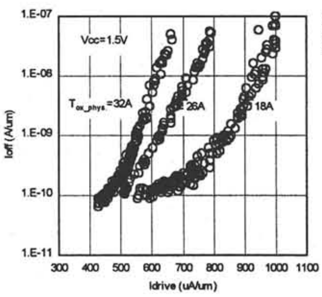

Fig. 8. Comparison of measured driving current versus off state current curves for n-FETs with various oxides thickness; Vcc=1.5V.

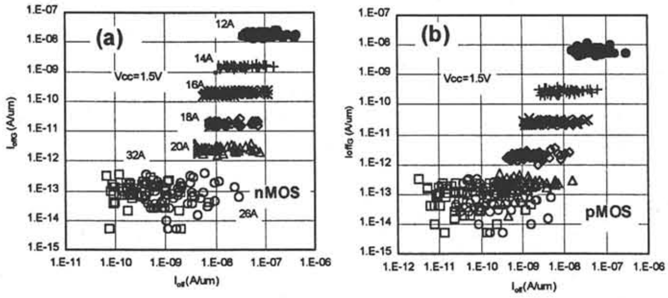

Fig. 7. Comparison of measured off state drain current (I_{off}) versus off state gate leakage (I_{offG}) curves for (a) n-FETs and (b) p-FETs with oxides ranging from 32 Å to 12 Å; V_{CC}=1.5V.

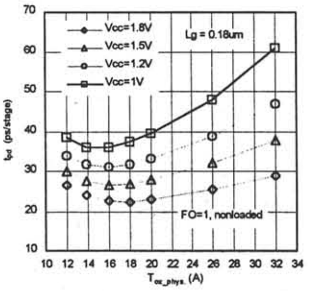

Fig. 9. Measured t_{pd} versus T_{ox_phys} with V_{CC} ranging from 1V-1.8V and oxides ranging from 32 Å to 12 Å.

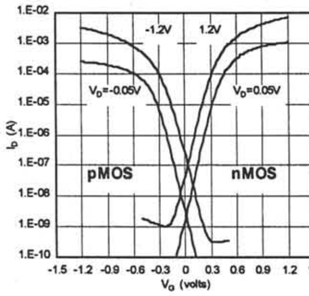

Fig. 10. I-V characteristics for 0.1μm n- and p-channel MOSFET; V_D=0.05 and 1.2V; T_{ox_phys} =18Å.