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Surface Channel Metal Gate CMOS with Light Counter Doping and Single Work Function Gate Electrode

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1. Introduction

Recent development of low power and high speed Si devices is requiring low threshold voltage *Vth* value with its small deviation, thinner effective gate oxide thickness and smaller parasitic capacitance in MOSFETs. Concerning these points, metal gate MOSFETs have several advantages, such as no gate depletion and lower aspect ratio in cross section, compared with silicide/poly-Si gates and polymetal gates [1][2]. However, the *Vth* of metal gate MOSFETs are 0.4-0.5V higher than those of dual gate poly-silicon MOSFETs, since the work functions of the metals are usually around the center of the Si band gap. In order to realize low *Vth* CMOS with which has gate electrode with single work function, counter doping [1] is considered to be necessary. However, experiences in buried channel poly-Si gate MOSFETs with counter doping tell us several disadvantages, such as degradation in subthreshold swing, short channel effect (SCE) and *Vth* deviations, in exchange for advantages of solving difference in work function.

This paper presents a new finding that the boundary of being surface channel with counter doping in single metal gate CMOS is around 0.4 V of *Vth*. Using results with in-house simulators, we found a guideline in designing channel profiles of metal gate CMOS with low *Vth*, steep subthreshold swing, suppression of *Vth* deviations due to SCE and channel impurity profile deviations caused by process deviations. Measured characteristics of MOSFETs fabricated with the guideline show improved characteristics as expected with the simulation.

2. Simulated Model

Metal gate MOSFETs were investigated using 2-D device simulation. Fig. 1 shows simulated nMOSFET. Work function of metal gate is assumed to be in the Si mid-gap, i.e., 4.6 eV. Fig. 2 shows the simulated channel profile, in which high concentration (5×10^{18} cm^{-3}) p-type profile suppresses SCE, where counter doped layer decreases *Vth*. Dependence of MOSFET characteristics on the counter doped layer depth *d* and concentration of counter doped layer *Nc* were investigated in order to improve device characteristics. Sensitivity of *Vth* to these parameters were also investigated using simulation to reduce deviations in *Vth*.

3. Simulation Results and Discussions

Fig. 3 shows electron distribution in the channel at *Vth* for different counter doping profiles. Surface peaked electron distribution in 0.4 V of *Vth* was obtained not depending on d. However the peak shifted into substrate in 0.3 V of *Vth*, resulting in significant increase of effective oxide thickness. Hence we intended to investigate cases with 0.4 V of *Vth*.

Fig. 4 shows simulated *Vth* as a function of counter doped layer concentration *Nc* in three cases of *d* :10, 25, 45 nm. As seen in Fig. 4, sensitivity of *Vth* to *Nc* increases when *d* is decreased. In the conditions where *Vth* values were 0.4 V, the sensitivity of *Vth* to a change of *Nc* was 4.8 mV/1% in the case of shallow *d* (10 nm), which was reduced to 2.2 mV/1% and 0.06 mV/1% in the cases of 25 nm and 45 nm, respectively. Dependence of *Vth* on *d* in the cases of *Nc* where *Vth* value becomes 0.4 V for each *d* in Fig. 4 is shown in Fig. 4. Sensitivity of *Vth* to *d* in high *Nc* case (5.7×10^{18} cm^{-3}) was 86 mV/nm, which was decreased in low *Nc* cases.

Fig. 6 shows *Id-Vg* characteristics of these three cases of channel profile with 0.4 V of *Vth*. As seen in Fig. 6, shallow *d* does not give good subthreshold characteristics, but deeper *d*'s give better ones due to the smaller capacitance between the channel and the substrate. However, larger *d* shows slight increase of subthreshold current, since SCE is not strongly suppressed. In Fig. 6, it is also seen that current in strong inversion range in the case of shallow *d* is degraded because of high concentration impurities. From the results of Fig. 4 to Fig. 6, light counter doping with deep profile is preferable concerning suppression of Vth deviation and better subthreshold swing. Fig. 7. shows SCE for the case of 25 nm of *d*. The estimated *Vth* deviation range caused by SCE in the change of gate length *L* by +/- 8% is also plotted in Fig. 7, which is 12.5 % of *Vth* at 95 nm of *L*. In designing channel profile of surface channel metal gate MOSFET, one should choose deep *d* within the range where SCE is effectively suppressed.

Because the work function of the metal of the simulated MOSFETs is assumed to be in the mid-gap, these discussions are also applicable to pMOSFET due to the symmetry. These guidelines are recommended as designing profiles of surface channel metal gate CMOS.

4. Device Fabrication and Measured Results.

Determining implantation conditions combining process and device simulations to obtain 0.4 V of *Vth* with the above guideline, the Damascene gate process was used in fabricating metal gate MOSFET[2]. Single metal with sputtering TiN was used as gate electrode for n and pMOSFETs. TEM and schematic cross sections of the fabricated MOSFET are shown in Fig. 8. Fig. 9 shows measured characteristics with $|Vd|$ = 0.05 V and 1.5 V with good subthreshold characteristics for nMOSFET with *L* of 150 nm and pMOSFET with *L* of 200 nm on a wafer.

Comparison of characteristics of devices with 500 nm of *L*, excluding effects from SCE, between two types of profiles is listed in Table I. Lower *Nc* case, which is from the same wafer as the case of Fig. 9, shows reduced subthreshold swing factor *S* and *Vth* deviation which is consistent with the simulation.

5. Conclusion

Metal gate CMOS which has light counter doping with appropriate depth within the range of suppressing SCE shows good electrical characteristics with steep subthreshold swing and small deviations in *Vth*. Lightly counter doped surface channel is promising in realizing low Vth metal gate CMOS.

References

[1] A. Chatterjee et al., IEDM98, pp. 777-780, 1998.
[2] A. Yagishita et al., IEDM98, pp.785-788, 1998.

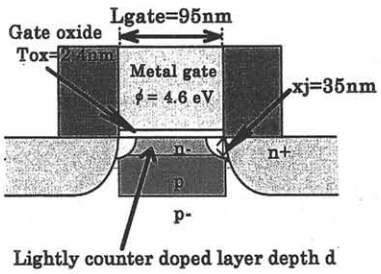

Fig. 1 Simulated nMOSFET. Channel dopants are locally introduced solely to the channel area, and are supposed to be implanted after the dummy gate removal in the Damascene gate process [2].

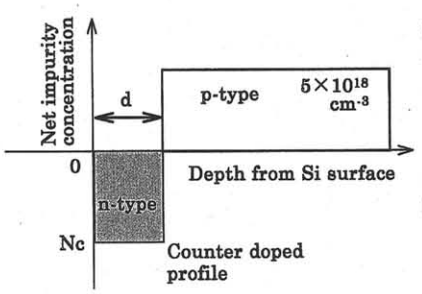

Fig. 2 Simulated box shaped profile of counter doped channel.

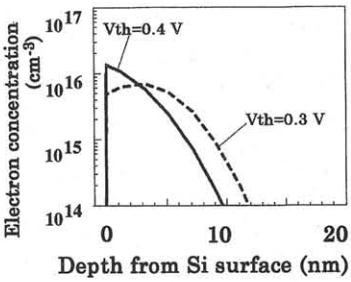

Fig. 3 Comparison of electron distribution at *Vth* in different counter doping profiles. *d*=25 nm.

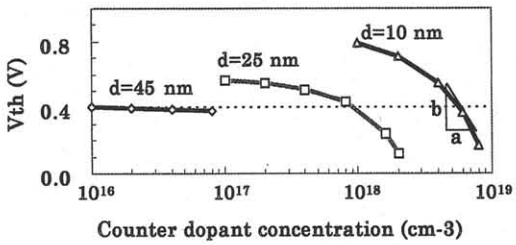

Fig. 4 Simulated *Vth* dependence on counter doped layer concentration *Nc*. Sensitivity in *Vth* on deviation of *Nc* is shown by b/a in the case of 10 nm of *d*, which is quite high.

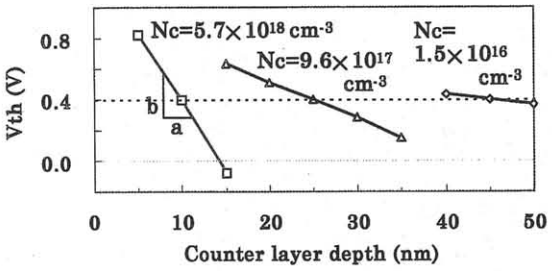

Fig. 5 Simulated *Vth* dependence on counter doped layer depth *d* in counter doped channel. Sensitivity in *Vth* to deviation of *d* is shown by b/a in the case of 5.7×10^{18} cm^{-3}, which is higher than other cases.

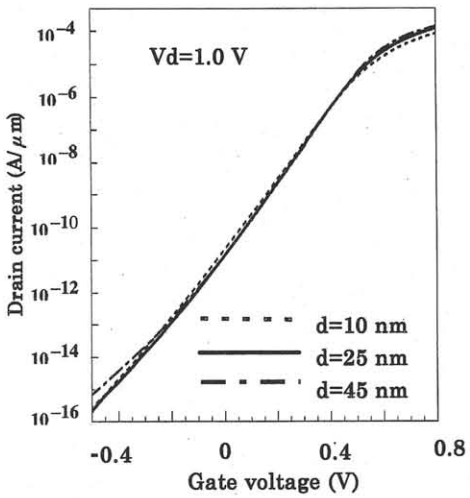

Fig. 6 Simulated *Id-Vg* characteristics dependence on counter doped layer depth *d*. 25 nm of *d* shows the best subthreshold characteristics, where 10 nm of *d* shows the worst.

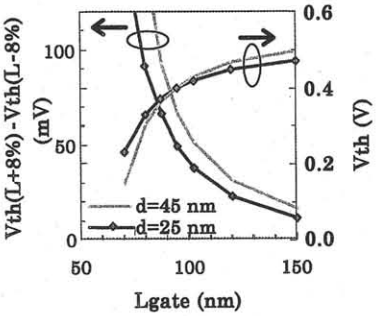

Fig. 7 Simulated short channel effect dependence on counter doped layer depth *d* of 25 nm and 45 nm. *Vth* deviation range in deviation of *L* in +/- 8% is also plotted. 25 nm of *d* shows small Vth deviation range in short channel effect.

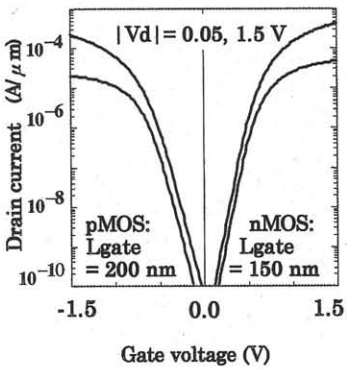

Fig. 9 Measured *Id-Vg* characteristics of the fabricated metal gate MOSFETs. As channel impurities, In in 150keV and As in 5keV of implantation energy, and B as halo impurity were used for nMOSFET. Sb 160 keV and B 5keV as channel impurities were used for pMOSFET.

Table I Measured characteristics of fabricated nMOSFETs

Nc (cm^{-3})*	Vth (V)	σ (Vth)(mV)	S(mV/dec)
2×10^{18}	0.44	13.6	78
5×10^{18}	0.42	16.4	81

*Peak concentration of counter dopant determined from SIMS profile.

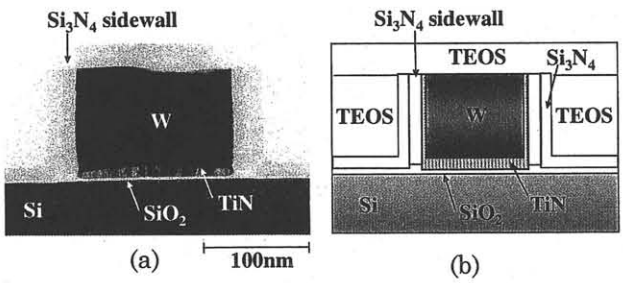

Fig. 8 (a) TEM cross section of fabricated metal gate MOSFET. (b) Schematic diagram of fabricated metal gate MOSFET.