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High Density 0.16 μm Embedded-DRAM-ASIC Process Technology for a SoC Platform

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Introduction

An embedded-DRAM-ASIC technology enables the implementation of more functions on a single chip and is a generic process technology for a system-on-a-chip (SoC) platform. In SoC, high density memory and logic are recognized as number-one-priority [1]. Also, low power, high speed, and cost are important issues of SoC when considering process architecture.

In this paper, we discuss the implementations of the high density and low power 0.16um embedded DRAM ASIC process. To achieve high density, the self-aligned contact (SAC) is a key technology to increase the DRAM macro, SRAM macro, and also logic densities. We highlight the transistor design issues related to the SAC technology for the first time. We also focus interconnect design to achieve high density and low power ASIC.

Process Integration

Figure 1 (a) and (b) show the cross sectional SEM views of the embedded DRAM cell part and high density logic part. The W-polycide dual gate is covered with the Si-nitride (SiN) film for the SAC. Only sources and drains of logic parts are salicided with CoSi2 (10Ω/sq.). Thin SiN films of the sidewall and the etch stopper are used for the SAC to the gate and to the field. W-bitlines are merged to local interconnects (LI) of logic parts. It is contributed to avoiding deep contacts of the first metal. And, its shallow contact of LI also makes ease of the SAC etching to the gate and to the field at logic parts. The 8F2 of 0.22um cylinder-type DRAM Cell (0.39um2) is integrated with the SAC and the aggressive SRAM cell (<4um2) is also realized with the SAC to the gate and the field. The logic gate density also becomes the high value up to 170kG/mm2 due to the SAC. Figure 2 shows a top view of 3.49um2 SRAM bit cell. The nominal interconnect option of one LI, three levels fine metals, and two levels rough thick metals is provided. The FSG and the aluminum are the standard option.

To integrate the SAC,W-polycide dual gate, CoSi2, and DRAM-cell, assignment of process windows for interdiffusions, boron penetrations, junction leakage are the critical issues [2-3]. Figure 3 shows the example of a process window on the interdiffusion. The threshold voltage shift is suppressed when the arsenic is chosen, and the temperature of the S/D RTA anneal and the furnace anneal which corresponds to the DRAM cell formation are restricted to be below 1000℃ and 800℃, respectively. The Vfb shift, shown in Fig.4, is reduced with the LPCVD-SiN film, compared with the PECVD-SiN film, which may be attributed to the enhancement of boron penetration by H2 in SiN films with the SAC, as also reported recently [2-3]. The low temperature MIS-DRAM-cell-formation also needs the care to suppress the depletion, shown in Fig. 5.

Transistor Design Issue Related to SAC Structure

The optimization of a halo and a extension implantation condition is a key issue to achieve a high performance transistor. Especially, the angle of a halo should be designed to be the allowed high angle to control the short-channel effect and concurrently to reduce junction capacitance, shown in Fig. 6. However, it is restricted by the height of the neighbor gate stack. Moreover, the height of the gate stack becomes higher when the SAC is adapted because the cover SiN film is also stacked on the gate. Therefore, we precisely check the allowed angle at the configurations of the nearest neighbor gate stacks by Monte-Carlo simulations. The stopping power of SiN , WSi2, and polysilicon films are precisely included in the model. The results show the 30 degree is acceptable at the gate space of 0.26um, and ions of the halo are blocked by the next gate stack below 0.26um, shown in Fig.7. It is also suggested by the Monte-Carlo that the stopping power of WSi2 film determines the extent of halo ions at channel center, which contributes to a reverse short channel effect .

Those suggestions are included at the transistor design. The dual gate oxides (4.0nm/7.5nm, electrical at inversion) are used. The thin oxide is for the logic of 1.8V and the thick oxide is for the DRAM cell and the 3.3V IO-interface. The Id-Vd characteristics of 0.16um MOSFET for the logic are shown in Fig. 8. The simulated tpd is 26pS, which is also attributed to the reduction of junction area with the SAC. They are not leading edge, however, have the competitive performance.

High Density and Low Power Interconnect Design

To reduce the routing grid of interconnection is a key issue for a high density ASIC. The end of the line rule (extension) which is generally adapted, enlarges the routing grid of a CAD-based-ASIC. Therefore, we introduced the optical proximity correction (OPC) at LI and fine metals to reduce the shortening of the line end, shown in Fig. 9. It also contributes keeping the electromigration resistance and the high yield in case of the misalignment and realizes 0.52um-ASIC-grid.

The W-bitline is used as the LI. The capacitance (Cw) of the LI is low because the film thickness is thin, compared with the aluminum. Its low Cw is beneficial from the viewpoints of tpd , shown in Fig.10, when the wire length is below 1mm, although the resistance (Rw) of LI is one order higher than that of the aluminum. Therefore, most of all logic cells can be drawn by LI, which results in the cost-effective.

The thickness of 3 levels fine metals are also designed, based on the consideration of Cw and Rw contribution to tpd. It results in that Cw reduction is more beneficial than the slight Rw increase. Moreover, both the introduction of the FSG and the slight reduction of the metal thickness result in that the Cw keeps constant, compared with the 0.25um generation, although the line & space reduced aggressively, shown in Fig. 11. It means that the power consumed at the interconnect is reduced directly by the scale factor.

The low CR interconnects for the global routing are provided at top 2 levels of the metals. The acceptable interconnect width (= 1um) is obtained, if the long line clock frequency is 300MHz which is the average target of 0.16um ASIC, shown in Fig.12.

Conclusions

The integration issues of high density 0.16um embedded DRAM ASIC process technology was shown. The transistor design related to the SAC structure and the high density and low power interconnect design was highlighted.

References

[1] R. Kramer, IEDM Tech. Digest, pp.3-7 ,1999
[2] M. Yoshida, et al., IEDM Tech. Digest, pp.41-44, 1999
[3] M. Togo, et al., IEDM Tech. Digest, pp49-52, 1999

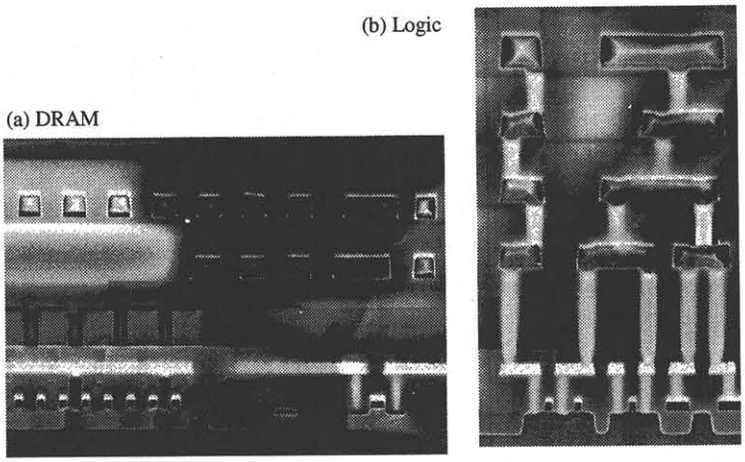

Fig.1 Cross sectional SEM views of the embedded DRAM cell part (a) and the logic part (b). Note: only 4 levels metals are shown.

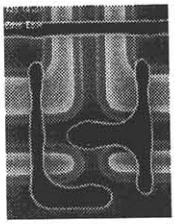

Fig. 2 Top view of aggressive 3.49um2 SRAM bit cell.

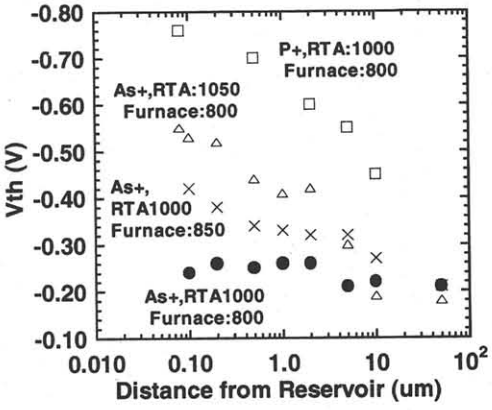

Fig. 3 Process window on interdiffusion. Vth of Pch MOSFET which are connected to N+ reservoir are shown.

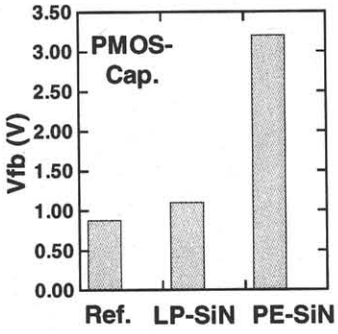

Fig. 4 Vfb of Pch MOS capacitor with various hard masks.

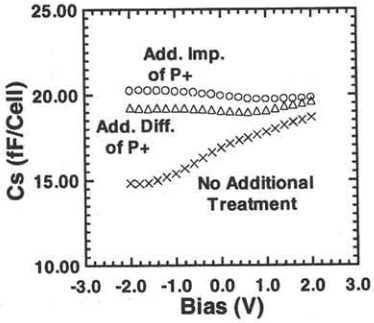

Fig. 5 Suppression of depletion on low temperature MIS capacitor. Temperature is restricted at 750 ℃. Additional Doping is necessary to suppress the depletion.

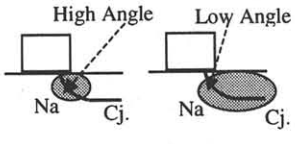

Fig. 6 Effect of halo angle. High angle makes low Na to control SCE. Low angle needs high Na and raise Cj.

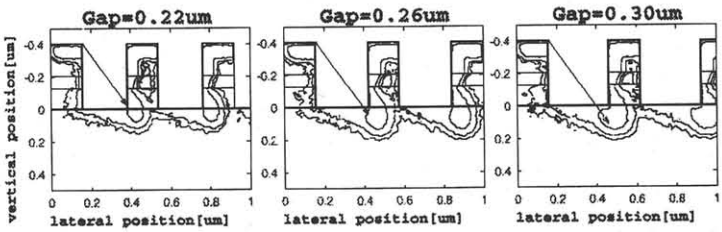

Fig. 7 Results of Monte-Carlo simulations. The channel profile at channel is the same when the gate space is larger than 0.26um. It is also determined by the stopping power of WSi2.

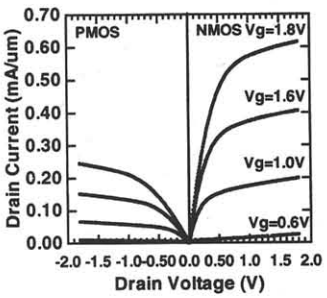

Fig. 8 Id-Vd characteristics of 0.16um MOSFET for Logic.

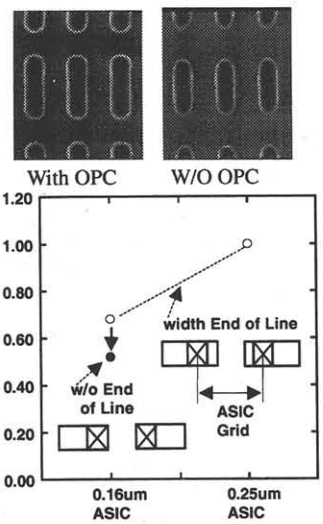

Fig. 9. ASIC metal grid with and without end of line. Reducing of shortening of line-end with OPC is also shown on top of figure.

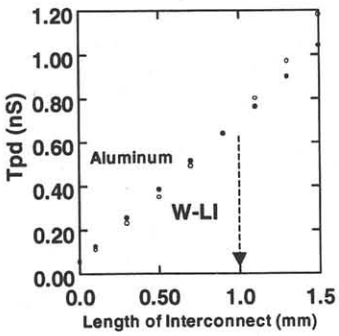

Fig. 10 Simulated tpd of wire load, aluminum vs W-LI. The latter is firster than the former below 1mm.

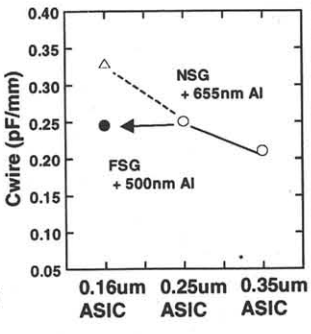

Fig. 11 Wire capacitance of 3 parallel lines. Metal grid of 0.16, 0.25, and 0.35 ASIC are 0.52um, 1.0um, 1.4um, respectively.

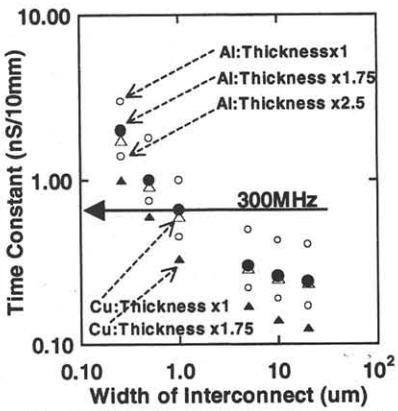

Fig. 12 Dependence of time constant of global wire on wire width. Al(500nm) x1.75 with width of 1um meets 300MHz at typical long line clock (20% of total tpd is assigned to be wire delay).