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70nm NMOSFET Fabrication with 12nm n^+-p Junctions Using As_2^+Å Low Energy Ion Implantations

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1. Introduction

In order to fabricate the nano-scale MOSFET devices, extremely shallow source/drain junctions are required to suppress the short channel effects [1, 2]. According to the ITRS`98 roadmap, source/drain extensions shallower than 30 nm will be required for 70 nm CMOS generations [3]. As_2^+ low energy ion implantation technology for shallow n^+-p junctions has been studied because of its lower effective acceleration energy, higher dose, controllable doping profile and low diffusion coefficient [4, 5]. As an alternative to the ion implantation technology, the solid phase diffusion and the plasma doping method have been investigated by many researchers. However, the solid phase diffusion process causes a complexity of the CMOS fabrication process and the plasma doping method generates an impurity and energy contamination problem. In this paper, we focused on the fabrication and characterization of the nano-scale NMOSFET with source/drain extension regions of the extremely shallow junction depths (12 nm) and the sheet resistance of 1.0 kΩ/□ using As_2^+ low energy ion implantation technology.

2. Experimental

The device fabrication sequence is summarized in Fig. 1. A retrograde channel doping profile was created by boron ion implantation through a sacrificial oxide of 25 nm. This was followed by the threshold voltage adjustment implantation with BF_2, the growth of the gate oxide, and the deposition of poly-Si. The gate structure consists of 3.5 nm gate oxide, 100 nm phosphorus doped poly-Si, and 50 nm TEOS hardmask. The size of the gate electrode was measured by using the cross-sectional SEM photographs. Then, poly-Si re-oxidation was carried out at 800 °C for 5 min. As_2^+ ion implantations for source/drain extension region formation were done at 5 keV or 10 keV with 5×10^{14} cm^{-2} by Varian A2F medium current/medium energy ion implanter through the screen oxide of 3.8 nm around a gate electrode. After 100 nm TEOS sidewall spacers were formed, the As^+ ion implantation was done for the deep source/drain formation. RTA (1000 °C, 5 sec) was performed to activate the implanted dopants as well as to cure the implantation damage. The dopant profiles were analyzed by SIMS and sheet resistance measurements.

3. Results and Discussion

12 nm n^+-p junctions with the sheet resistance of 1.02 kΩ/□ are implemented by the As_2^+ 5 keV ion implantation. Smaller sheet resistance of 0.45 kΩ/□ is obtained in the As_2^+ 10 keV ion implantation at the same RTA condition. An average doping concentration of the n^+ region is measured to be about 3.3×10^{20} cm^{-3}. Fig. 5 shows the I_D-V_G, I_D-V_D characteristics of the L_{gate} = 70 nm NMOSFET with the As_2^+ 10 keV ion implantation. Fig. 6 shows the V_T roll-off characteristics for As_2^+ 5 keV and 10 keV implanted NMOSFETs. The higher DIBL of 150 mV is observed in the 10 keV NMOSFET device. While the NMOSFET with the 10 keV ion implantation process shows a significant V_T degradation around the L_{gate} of 100 nm, the V_T roll-off of NMOSFET with the 5 keV ion implantation process exhibits a smaller V_T roll-off. This immunity to short channel effect is due to smaller side diffusion under the gate electrode. NMOSFET fabricated by 5 keV ion implantation shows the maximum transconductance of 337 mS/mm for the L_{gate} = 100 nm NMOSFET at a drain voltage of 1.5 V, compared with the NMOSFET of As_2^+ 10 keV ion implantation with 405 mS/mm. This current drivability difference is due to the increased resistance of source/drain extension regions formed by lower ion implantation energy.

4. Conclusions

In conclusion, As_2^+ low energy (≤10keV) ion implantation technology realizes the ultra-shallow junction of 12 nm and the high doping concentration of about 3.3×10^{20} cm^{-3}. The NMOSFET with ultra-shallow junctions formed by this low energy As_2^+ ion implantation provides a reduced short channel effect. With further careful process optimization or advanced device structure, As_2^+ low energy ion implantation technology will show the promise of the better performance of NMOSFET with extremely shallow junctions.

Acknowledgements

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References

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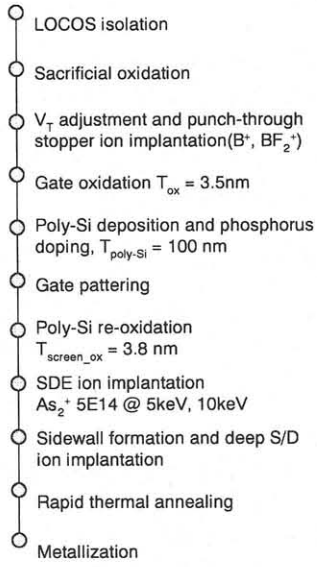

Fig. 1. Key process steps to fabricate the NMOSFETs with ultra shallow n^+-p junctions using As_2^+ low energy ion implantations.

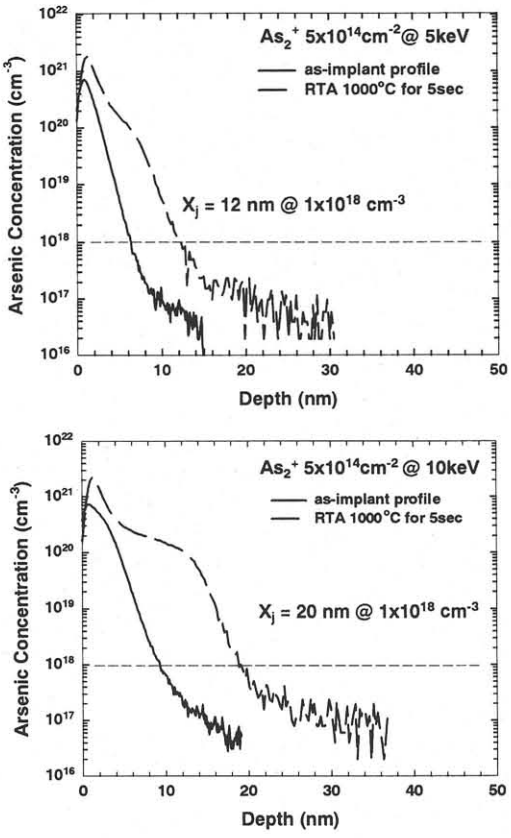

Fig. 2. As-implanted and post-RTA SIMS profiles of arsenic. Because SIMS analysis for as-implanted arsenic profiles was carried out without screen oxide strip, an arsenic concentration at silicon surface regions was measured with the small transient error of SIMS measurement system.

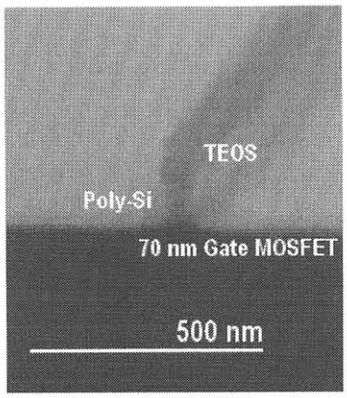

Fig. 3. The cross-sectional SEM photographs of 70 nm gate length NMOSFET

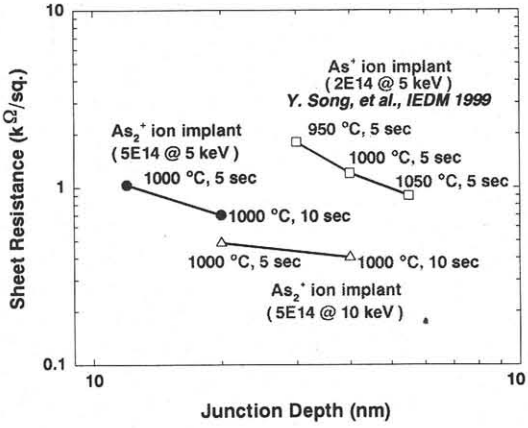

Fig. 4. Sheet resistance versus junction depth for As ion implantation process.

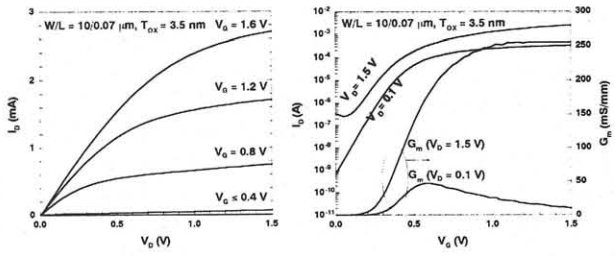

Fig. 5. The I_D-V_G and I_D-V_D characteristics of fabricated NMOSFETs with gate length of 70 nm.

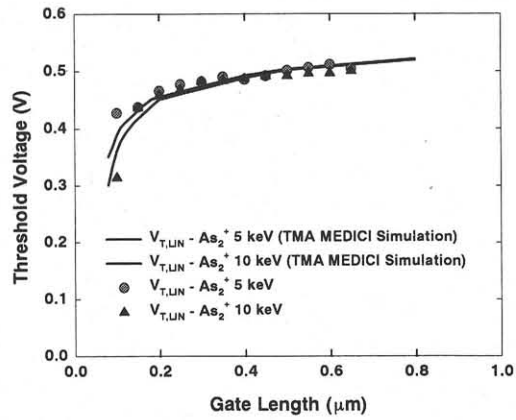

Fig. 6. The improved threshold voltage roll-off characteristics are achieved in the As_2^+ 5 keV NMOSFETs.