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# Self-Aligned Pocket Implantation into Elevated Source/Drain MOSFETs for Reduction of Junction Capacitance and Leakage Current

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## 1. Introduction

Further scaling-down of CMOS technology requires shallower source/drain (S/D) junction together with highly-doped and/or non-uniformly-doped channel for minimization of short channel effects. However, they inevitably cause an increase of parasitic S/D resistance, junction capacitance, and current leakage, which degrade static and dynamic MOSFET performance. One of the practicable methods for overcoming these problems would be introduction of a S/D elevation technique into MOSFET fabrication process [1-4]. In this work, self-aligned pocket implantation through the elevated Si epitaxial layer was newly demonstrated so as to reduce the parasitic capacitance along with the leakage current without any influence on the short channel behaviors. The significant effects due to modification of the pocket-doped impurity profiles were experimentally and simulationally confirmed.

## 2. Experimental Procedure

The CMOS process sequence involving the elevated S/D technique was depicted in Fig. 1. After formation of conventional shallow trench isolation and retrograde well, poly-Si gates were patterned on gate insulator of 2.8 nm thick, and stacked $SiO_2$ (94 nm)/$Si_3N_4$ (6 nm) sidewall was formed. The deep S/D implantation followed and the Si selective epitaxial growth utilizing ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) was carried out [5]. The thickness of the epi-Si layer on the $n^+$ region was about 40 nm, whereas that on the $p^+$ region was found to be thinner. Then the epi-layers were doped by additional As or $BF_2$ ion implantation. After removal of the outer $SiO_2$ sidewall, S/D extension and pocket implantation were performed through the $Si_3N_4$ film and the epi-Si layer. As control samples, non-elevated $p$ and $n$MOSFETs were prepared through the similar manner without the selective epitaxial growth.

Scanning electron microscope image of the fabricated $n$MOS whose gate length is about 30 nm is shown in Fig. 2. The surface morphology of the epi-Si layer is very smooth, which indicates superiority of the present selective epitaxial growth technique.

## 3. Results and Discussion

Figures 3(a) and (b) show simulated distribution of the pocket-implanted boron after appropriate thermal treatment for the elevated and the non-elevated S/D $n$MOSFETs, respectively. Although the boron impurities are successfully implanted into the pocket positions to suppress the short channel effects, its profiles under the elevated regions shift to upper positions since the pocket-implantation was performed through the epi-Si layer. Therefore the boron concentration around the $pn$ junction in the elevated S/D $n$MOS becomes lower, which strongly suggests smaller parasitic junction capacitance.

Figures 4(a) and (b) show the experimental and the simulated deep S/D junction capacitance dependence on the drain voltage. Taking advantage of the elevated configuration appreciably reduces the junction capacitance, and the effect is especially greater in the $n$MOS than in the $p$MOS. This would be due to the differences in not only the epi-Si layer thicknesses but also the pocket/channel impurity profiles.

The junction leakage current is also suppressed by the S/D elevation as shown in Figs. 5(a) and (b). Particularly, significant effect is obtained in $n$MOS. It is interpreted in terms of the weakened internal junction electric field, which is similar to the $C$-$V$ results mentioned above.

The short channel characteristics are compared in Figs. 6(a) and (b). Good behaviors are attained without any remarkable differences between the elevated and non-elevated devices. This implies that the doping profiles at the extension regions are similar in both of them in spite of the elevation of the deep S/D regions, as pointed out in Fig. 3.

Figures 7(a) and (b) show the $I_{on}$-$I_{off}$ characteristics. Drivability is appreciably improved by the S/D elevation, which is due to the reduction in the S/D sheet resistance.

## 4. Conclusion

An elevated S/D technology combined with self-aligned pocket implantation was investigated in detail. The experimental data revealed that the significant improvements in the junction capacitance as well as in the junction leakage were achieved without any degradation in the short channel characteristics. They were supported well with the simulation study and should be explained in terms of the modification of the pocket-doped impurity profiles at the deep S/D regions.

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## References

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Fig. 1 Process flow.

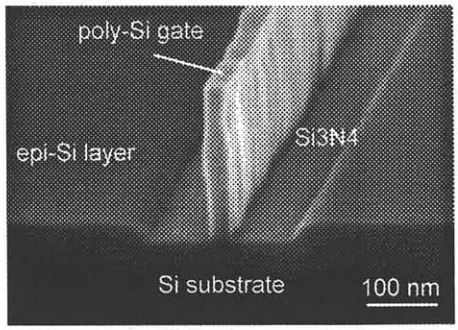


Fig. 2 Cross sectional SEM image of the elevated S/D transistor.

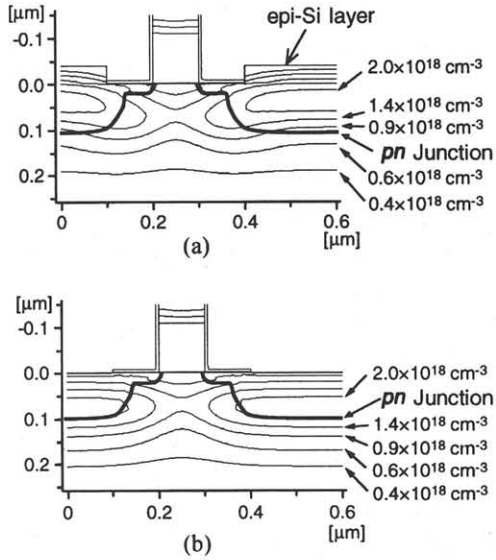


Fig. 3 Simulated B profiles and ***pn*** junction boundary (***n***MOS), (a) Elevated S/D, (b) Reference.

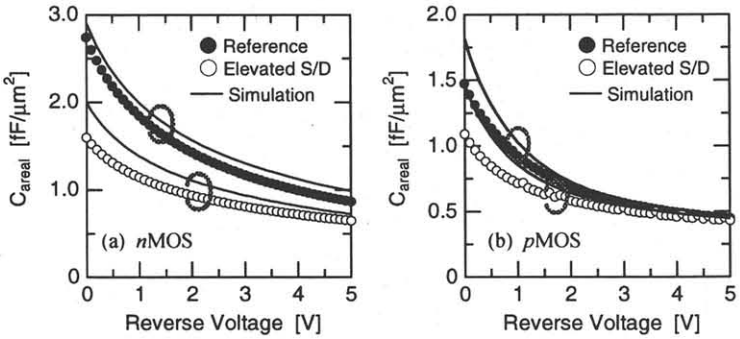


Fig. 4 Junction capacitance dependence on reverse drain voltage, (a) *n*MOS, (b) *p*MOS.

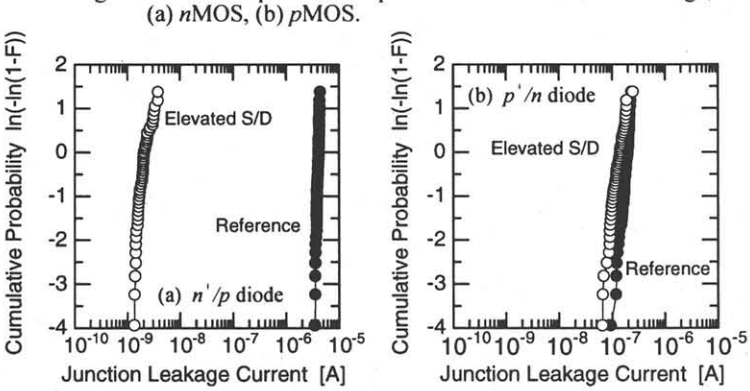


Fig. 5 Junction leakage characteristics, (a) *n*MOS, (b) *p*MOS.

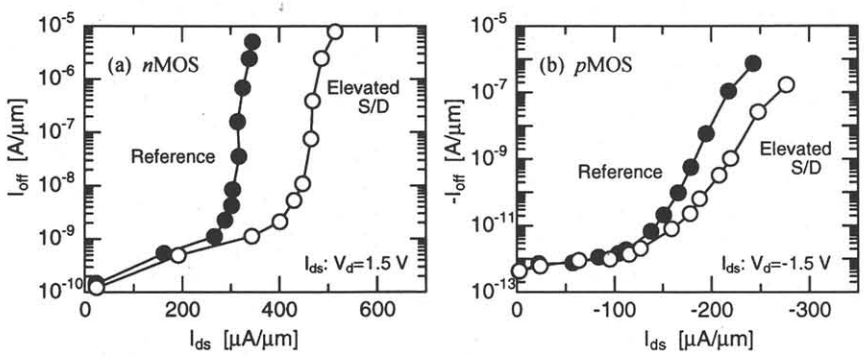


Fig. 7 $I_{on}$-$I_{off}$ characteristics, (a) *n*MOS, (b) *p*MOS.

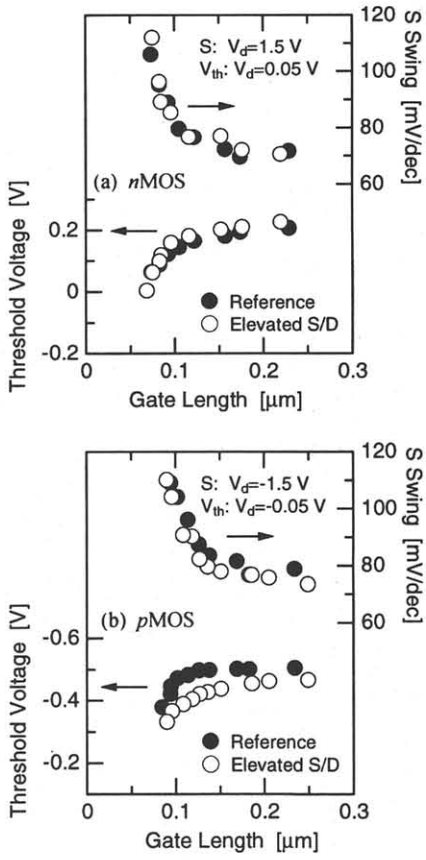


Fig. 6 Short channel characteristics, (a) *n*MOS, (b) *p*MOS.