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A Novel T-Shaped Shallow Trench Isolation Technology Using Sidewall Spacer for 512Mbit Flash Memories and Beyond

S.H. Hong, D.H. Ahn, M.H. Park, T.K. Kim, H.K. Kang, and J.T. Moon
Semiconductor R&D Center, Samsung Electronics Co., LTD
San #24, Nongseo-Ri, Kiheung-Eup, Yongin City, Kyungki-Do, 449-900, Korea
Tel.:82-2-760-6322, Fax.:82-2-760-6299, Email:shhong48@samsung.co.kr

Abstract

This paper describes a novel T-shaped Shallow Trench Isolation (STI) technology which has the same effective isolation length with conventional STI and dramatically lowered aspect ratio. We adopt this technology to 512 Mbit flash memory and ensure excellent structural and electrical properties. And then we obtain the excellent gap filling ability even in 1 Gbit flash memory and beyond.

Introduction

In coming digital era, the need of high density flash memory become bigger and bigger. So, isolation technology is swiftly transforming from LOCOS to STI to fulfill the need of high density devices. But, conventional STI has also problems such as void free gapfill, gate oxide integrity and CMP planarization [1]. Especially, trench fill without void is a critical problem because flash memory has line-type cell layout. In this paper, by changing of trench shape, We propose a new isolation structure with lower aspect ratio but same trench depth. It can be used for 1 Gbit level flash memory.

Capability limitation of the Gapfill

Fig. 1 shows the relationship between the aspect ratio increasing and the gapfilling ability of O_3 TEOS Undoped Silicate Glass (USG) and High Density Plasma (HDP) in proportion as flash memory gets more integrated. According to this graph, O_3 TEOS USG can fill up to 256 Mbit has aspect ratio 2:1, HDP can fill up to 512 Mbit has aspect ratio of 3:1. For the case of beyond 1Gbit design rule, BPSG and poly silicon filling method are examined to solve filling problem. But it also has to solve device influence and stress increasing problem [2], [3].

T-shaped STI fabrication process

The schematic of proposed T-shaped STI is outlined in Fig. 2. After active definition, 0.15㎛ deep 1st trench is formed. The depth of 1st trench is shallow enough to fill it using USG/ HDP. After 180㎚ thick oxide deposition, oxide spacer is formed (Fig. 2 (a)). The thickness of spacer will be defined the width of 2nd trench. 0.25㎛ deep 2nd trench is etched using oxide spacer mask (Fig. 2 (b)) and oxide spacer is removed by wet etching (Fig. 2 (c)). After T-shaped trench is formed, trench oxidation, gapfill with USG or HDP oxide and CMP process for planarization are performed respectively. Finally stack layer is removed by wet etching (Fig. 2 (d)).

Physical Characteristics

Fig. 3 shows the SEM photograph of conventional & T-shaped STI. In spite of the same trench depth, T-shaped STI is completely filled with USG and void within 2nd trench will not affect device characteristics. The reason why there is superior gapfilling ability in T-shape STI is examined by CVD simulation. In gapfilling process, void is made due to the overhang of CVD oxide. To increase the aspect ratio, void by overhang is become larger and located in STI surface. T-shaped STI, however, void is only located in narrow 2nd trench and effective aspect ratio is limited to 1st trench depth. Consequently, T-shaped STI has superior gapfill property. Stress that is concentrated on the concave trench profile in T-shaped STI process is simulated by T-SUPREM 4 (Fig. 4). New stress concentrating points are generated at the 1st trench corner. But, the stress level is not enough to make a defect such as dislocation and the stress level at interface between silicon and field oxide is similar to that of conventional STI.

Electrical Characteristics

Fig. 5 shows the characteristics of N^+/N^+, P^+/P^+ BVDSS. There are no different punchthrough characteristics between T-shaped and conventional STI. Fig. 6 presents device simulation results of the E-field characteristics according to Vd. T-shaped STI has a isolation strengthening effects because of the narrow depletion width. The reason is that the doping level in this region is increased by T-shaped trench profile. Junction leakage curve is shown at Fig. 7. The stress level in STI is not quite different, so junction leakage is similar to that of conventional STI. In T-shaped STI processes, oxide undercut is formed when oxide spacer is wet striped. The effect of undercut is examined by Gox integrity and transistor characteristics as shown in Fig. 8 and 9. The level of Gox breakdown is similar to that of normal STI, and it cannot be shown hump in transistor operation. The effect of undercut to electrical characteristics is negligible. We applied this technology to 1 Gbit flash memory. Fig. 10 shows its result. The filling ability of T-shaped trench is better than conventional STI, of which the cell pitch and aspect ratio are 0.34㎛ and 3:1, respectively.

Conclusions

In this paper, a novel T-shaped trench isolation technology is adopted to 512Mbit NAND flash memory. The filling of STI in flash memory is more difficult than other devices because of line-type cell layout. However, we solved this problem through the change of STI profile. As far as there is no breakthrough in gap filling material, We believe this technology will be a strong candidate for ULSI isolation.

References

[1] Laura peters, Semiconductor Int. p.69, April, 1999
[2] T. Ukeda et al., Ext. Abs. of SSDM. p.260, 1996
[3] T. Cheng et al., Ext. Abs. of SSDM. p422, 1996

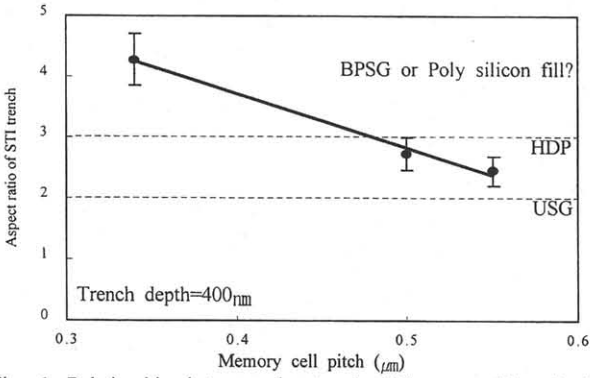


Fig. 1 Relationship between the trench filling material and the aspect ratio according to device scale down. Dotted lines are limitations of gapfill with HDP and USG.

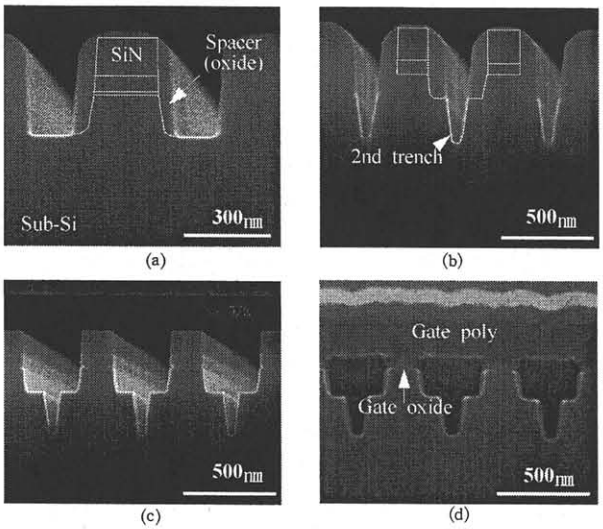
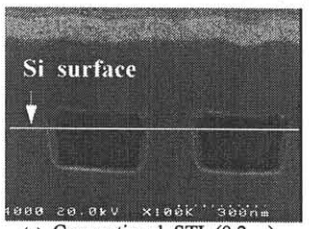
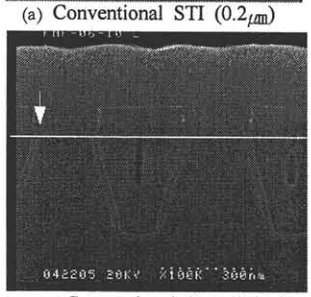


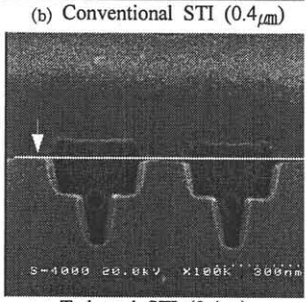
Fig. 2 The process flow of T-shaped STI. (a) active definition and spacer formation (b) 2nd trench etch, (c) spacer wet stripped, (d) after trench filling, CMP, gate-poly deposition.



(a) Conventional STI (0.2㎛)



(b) Conventional STI (0.4㎛)



(c) T-shaped STI (0.4㎛)

Fig. 3 Final profiles of T-shaped STI and conventional STI.

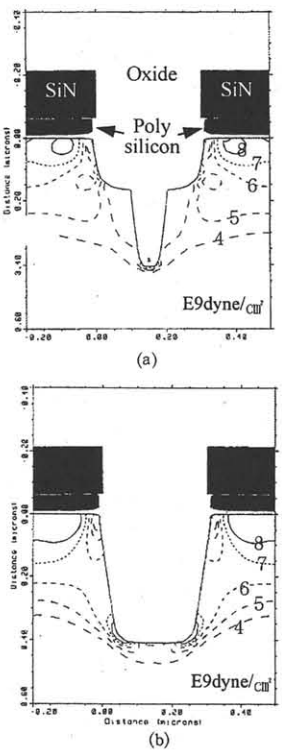


Fig. 4 Simulated shear stress contour of (a) conventional STI and (b) T-shaped STI.

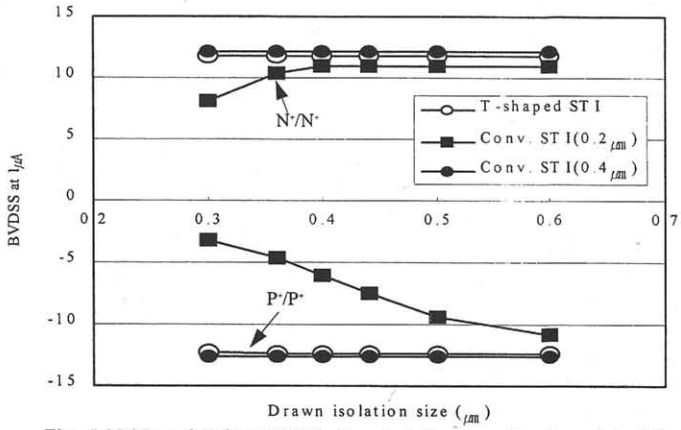
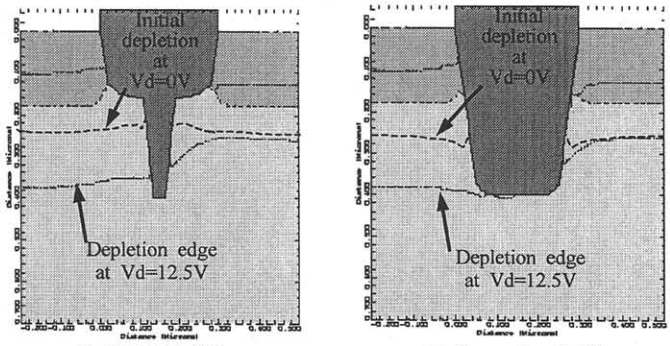
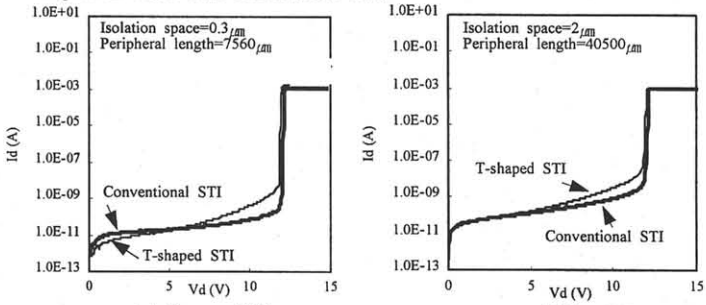


Fig. 5 N^+/N^- and P^+/P^- BVDSS characteristics as a function of isolation spacing.



(a) T-shaped STI (b) Conventional STI

Fig. 6 Simulated depletion characteristics according to drain voltage. Because of T-shaped trench profile, T-shaped STI shows narrow depletion width than conventional STI.



(a) Narrow STI (b) Wide STI

Fig. 7 Junction leakage characteristics according to isolation space with T-shaped STI and conventional.STI.

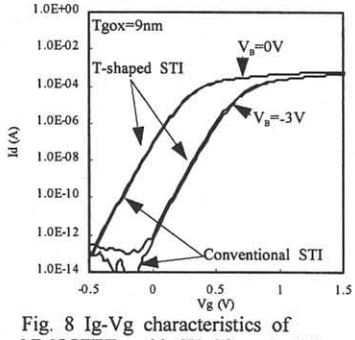


Fig. 8 Ig-Vg characteristics of NMOSFETs with W=20㎛, L=0.5㎛.

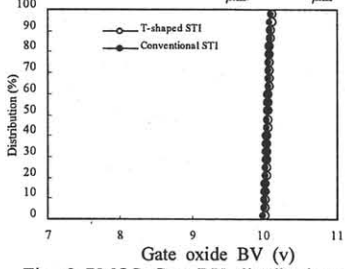
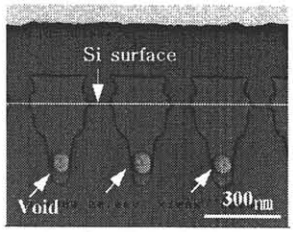
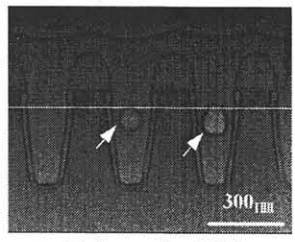


Fig. 9 PMOS Gox BV distributions at Ig=1㎂(Area=400*250㎛²).



(a) T-shaped STI



(b) Conventional STI

Fig. 10 SEM photographs of the worst case of gap-fill with HDP oxide. Memory cell pitch and aspect ratio are 0.34㎛ and 4.3, respectively.