Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 56-57

B-2-1 (Invited)

20nm MOS Devices for the Birth of the 21st Century

Simon Deleonibus, Guillaume Bertrand, Georges Guegan,
Michel Heitzmann, Pierre Mur, David Souil, Serge Tedesco.

LETI (CEA-GRENOBLE) Département de Microélectronique
17 rue des Martyrs 38054 Grenoble Cedex 09 France
Phone : +33 476 88 59 73 Fax :+33 476 88 54 59 e-mail : sdeleonibus@cea.fr

Abstract

Low voltage, low power and high performance are the great challenges for engineering of sub- 0.10μm gate length MOS devices. The possible options are reviewed through the issues in gate/channel and substrate, source and drain, gate dielectric engineering and alternative architectures. LETI realized in June 1999 20 nm finished gate length functional n channel MOS devices, the shortest devices ever realized by a conventional architecture.

1. Introduction

The projected evolution of the International Technology Roadmap for Semiconductor (ITRS)[1] (Table I) shifts the scaling to lower dimensions by two years as compared to the 1994 predictions. For the first time, showstoppers other than lithography and interconnects issues appear to be deserved special attention: breakthroughs or evolution especially in design could be required.

Which are the main showstoppers for CMOS scaling? In our work, we focus on the possible solutions and guidelines for research in the next years in order to propose solutions to enhance CMOS performances before we need to skip to alternative devices. In other words, how can we offer a second life to CMOS ?

In order to address these questions, a "PLATO (Plateforme Technologique Ouverte) Microélectronique du Futur" program has been set up in France by LETI. It focusses on three main activities: 1) Ultimate CMOS 2) Alternatives to CMOS devices 3) Technological breakthroughs for sub 0.10μm CMOS. In this program, researchers coming from LETI, CEA, the industries, universities and the French CNRS are involved in the various projects.

The PLATO program is now operational: 20 nm finished gate length n channel MOSFETs (Fig. 1a) have been achieved last June 1999 in LETI in the 200 mm diameter Si wafers clean room[2]. Ultra thin 1.2nm silicon dioxide is used as gate insulator for these devices(Fig. 1b). 17nm deep shallow source and drains extensions are achieved by using 3keV $1x10^{14}at.cm^{-2}$ Arsenic implant and RTP activation(Fig. 2). 25 nm devices show a good Ion/Ioff 550μA/μm/30μA/μm trade-off whereas 20nm devices demonstrate high punch through current because of the very short channel length [2](Fig. 3) despite BF_2 halo implant. Field effect is still controllable on 20 nm gate length devices with estimated 4 nm metallurgical channel length: this characteristics can be observed by action on the gate(Fig. 3a) as well as on the bulk of the devices. The performances and the Ion/Ioff ratio of Lg=25 nm gate length devices can be improved at low temperature suggesting that carrier surface scattering and series resistance limits the transport properties at 77 and 293K[3](Fig. 4). Halo implant reduces efficiently limit short channel effects with minor impact on junction capacitance.

Table I nMOSFET parameters. Deduced from ITRS roadmap 1999[1]

Year in production	**2005**	**2008**	**2011**	**2014**
Lg(nm) dense lines	100	70	50	35
Lg(nm) MPU	70	50	35	25
Max.XjSD(nm)	100	70	50	35
Max. Xjext(nm)	25-40	20-30	13-20	10-15
Tox or EOT(nm)	2	1.5	1	0.6
VT(V)	0.40	0.40	0.20	0.1
Vsuppl(V)	1.5	1	0.50	0.3
Nave($x10^{18}cm^{-3}$)	1.2	2.5	4	6
Ncarriers in channel	600	350	180	90
Ion NMOS(μA/μm)	750	750	750	750
Wdepl(nm)	29	20	16	13
Nimpurities(L=Wmin)				
Dense lines-MPU	239-348	150-239	96-150	55-96

2. Conclusion

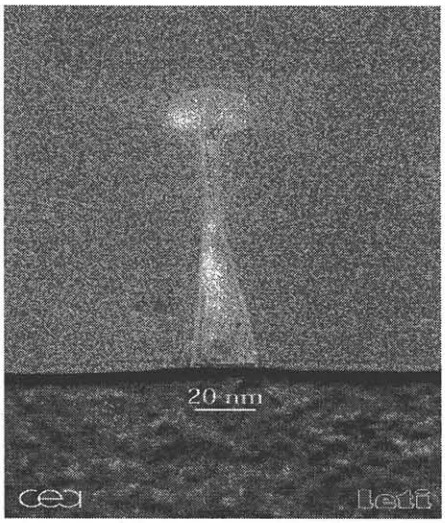
We achieved 20 nm gate length n-channel MOSFETs We are able to evaluate CMOS devices that will be fabricated beyond the limit of today's ITRS.

References

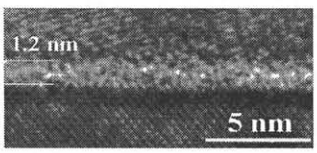
[1] The International Technology Roadmap for Semiconductors : Technology needs (1999 edition).

[2] S. Deleonibus et al. *IEEE Electron Dev. Letters, pp173- 175, April 2000.*

[3] G.Bertrand et al., Silicon Nanoelectronics Workshop 2000, pp.10-11, June 10-11, 2000, Honolulu(HI)

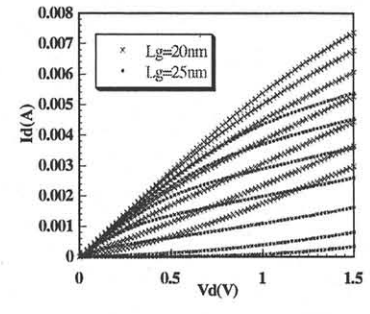


a)

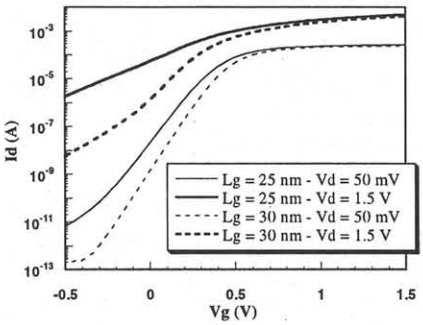


b)

Figure 1 a) TEM cross section of a 20 nm finished gate length device b) HR TEM of the 1.2 nm gate oxide[2]



(a)



(b)

Figure 3 (a) Id(Vd) characteristics for 25nm and 20nm finished gate length MOS transistors. The metallurgical channel length of the 20nm device is 4 nm[2]Gate oxide is 1.2nm thick SiO2. (b) Id(Vg) subthreshold characteristics for 25 and 30nm finished gate length MOS devices with the same characteristics as in (a)[2].

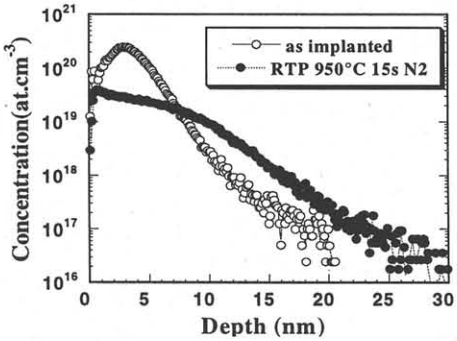


Figure 2 SIMS profile of extensions as implanted (open symbols) and after Rapid Thermal Annealing (closed symbols).

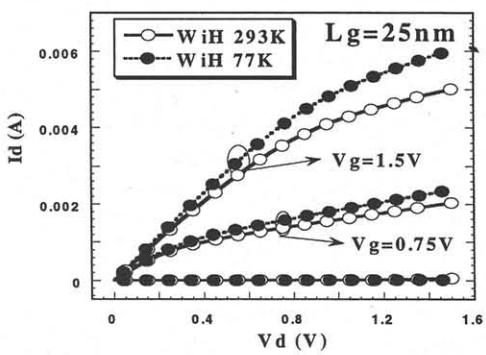


Figure 4 Id(Vd) characteristics for Vg=0; 0.75 and 1.5V at 293 and 77K of Lg=25 nm devices[3]. Source and drains architecture includes BF2 pockets

Acknowledgements This work has been carried out with PLATO Organization teams and tools in the frame of the "Ultimate CMOS project.