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A Study of the V_{TH} Fluctuation for 25nm CMOS

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1. Introduction

It is widely recognized that, for bulk CMOS, dopant-induced threshold voltage fluctuation may set a limit to the miniaturization, and that the use of intrinsic channel SOI (IC-SOI) can be a solution to this problem. However, though there are several attempts to determine dopant-induced V_{TH} standard deviation (σ_{VT}), the minimum attainable channel length for bulk is not clear because the acceptable σ_{VT} value is not clear. As for IC-SOI, V_{TH} fluctuation due to SOI thickness (T_{SI}) variation, which can be a serious issue, is not fully investigated. In an attempt to answer the above questions, bulk and planer/vertical IC-SOI MOSFETs are evaluated and compared from the viewpoint of V_{TH} fluctuation. The advantage of vertical SOI structures is discussed.

2. Bulk MOSFETs

6T-SRAM was used as a measure of σ_{VT} impact, as described below, since it is a typical logic component sensitive to the dopant-induced fluctuation. Fig.1 shows the equivalent circuit of a 6T-SRAM during read operation. To avoid flipping of the stored date by the reading, the static noise margin (M) must be larger than a certain value even if the V_{TH} values of the six transistors deviate from the designed ones (Fig.2). Keeping this condition satisfied, the worst case decrease of the read current (I_{READ}) was evaluated. For this purpose, M and I_{READ} as functions of V_{TH} deviation ΔV_i ($i = A_0, D_0, P_0, A_1, D_1, P_1$) were calculated using circuit simulation (Fig.3). Then, ΔM and ΔI were approximated as equal to linear functions u and v of ΔV_i (Fig.4), so that they can be easily calculated for any combination of ΔV_i. The linear approximation facilitates the statistical manipulation, since if V_{TH} is normally distributed, so are u and v.

Fig.5 shows dopant-induced V_{TH} standard deviation (σ_{VT}) for square (L=W) FETs vs. L, predicted by dopant number model[1] and percolation model[2], which tends to be optimistic and pessimistic, respectively. For L below 80nm, T_{OX} and V_{DD} are fixed at 1.5nm and 1V, to avoid too much gate leakage. Though constant T_{OX} causes the sharp rise of σ_{VT} in Fig.5, it should be noted that this does not worsen the situation, since the increase rate of σ_{VT}/V_{DD} is relieved by the fixed V_{DD}. Fig.6 shows estimated worst-case I_{READ} vs. L, assuming that ΔV_i is normally distributed, and the worst deviation of u and v is 6σ. V_{TH} of A_0 and A_1 is adjusted to secure 50mV noise margin, if it becomes necessary (Fig.6 dotted lines). Fig.6 shows that SRAM yield will approach zero around L=30nm due to the existence of extremely slow cells. Though the normality assumption needs further verification, it is likely that bulk CMOS suffers from the serious limitation at L=25nm.

3. Intrinsic Channel SOI MOSFETs

For intrinsic channel SOI (IC-SOI), V_{TH} fluctuation due to the T_{SI} variation, which is absent in bulk FETs, must be considered. It is caused, not by the dopant area density modulation (Fig.7a), as in doped FD-SOI, but mainly by 2D electrostatic effect (Fig.7b). Therefore, $\Delta V_{TH}/\Delta T_{SI}$ is correlated, to some extent, with short channel effect. Fig.8 shows simulated $\Delta V_{TH}/\Delta T_{SI}$ ($\equiv K_T$) and $\Delta V_{TH}/\Delta L$ ($\equiv K_L$) for various 25nm single and double gate IC-SOI FETs. Since all the calculations are for $T_{SI} \geq 7$nm, V_{TH} increase due to the quantum size effect[3] is ignored. It was found that, for single gate SOI, applying appropriate back bias minimizes both K_T and K_L (Fig.9). This can be accounted for by the bias dependence of the back channel and 2D effect. To suppress K_T and K_L, double gate structure, or thin buried oxide (BOX) with moderate back bias, or strong back bias is necessary, in addition to a very thin Si layer (~10nm). The double gate structure is most effective for suppressing not only K_L but also K_T.

Let us now compare (A) a planer single gate SOI with optimum V_{BACK}=-2V, and (B) vertical double gate SOI (Fig.10)[4]. Corresponding plots are labeled in Fig.8 (T_{SI}=10nm and L=25nm). To suppress the V_{TH} spread, $\Delta V_{TH}=K_T\Delta T_{SI}+K_L\Delta L$ should be minimized. For (B), moderately small ΔV_{TH} of around $\pm$80mV is obtained, even assuming relatively large ΔT_{SI} of $\pm$2.5nm (10% of L; for vertical SOI, larger ΔT_{SI} is expected, since T_{SI} is determined by lithography). However, for (A), to achieve similar ΔV_{TH}, ΔT_{SI} must be $\pm$1nm, because of the larger K_T value (Table 1). Though this ΔT_{SI} may be possible[5], considering all the tighter requirements for the planer single gate SOI (ultra-thin BOX (~10nm), ΔT_{SI} control of $\pm$1nm, necessity of relatively large V_{BACK}), vertical double gate SOI seems to be more attractive as a candidate for 25nm CMOS.

Fig.11 shows I_{READ} vs. L for the vertical SOI, translated from the results in Table 1. In this case, the worst case corner points are used. At L=25nm, V_{TH} fluctuation of the vertical double gate SOI will be still acceptable, in contrast to the bulk, assuming the reasonable ΔT_{SI} range.

4. Conclusion

Dopant-induced V_{TH} fluctuation will cause the failure of 25nm bulk CMOS SRAM, as long as the normality assumption is valid, and hence, IC-SOI will become necessary. Considering both $\Delta V_{TH}/\Delta T_{SI}$ and $\Delta V_{TH}/\Delta L$ characteristics, vertical double gate IC-SOI is attractive for 25nm CMOS, because of its high immunity against T_{SI} variation.

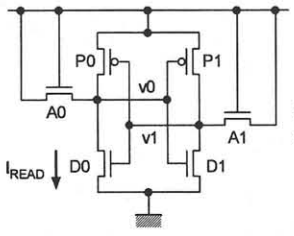


Fig.1 Equivalent circuit of SRAM during read operation.

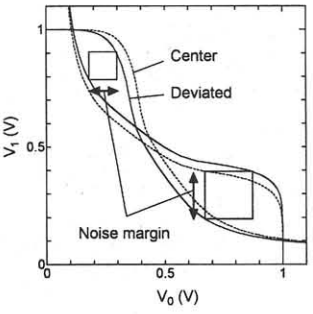


Fig.2 Static noise margin when V_{TH} deviation occurs.

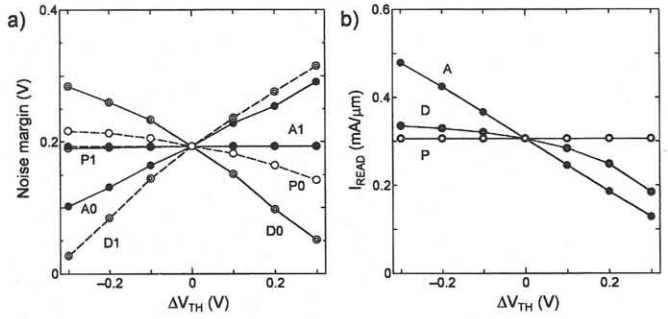
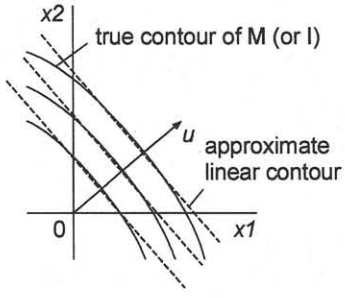


Fig.3 Response of static noise margin (M) and read current (I_{READ}) to V_{TH} deviation. W=2L for A_i and W=L for the rest. V_{TH} of one of the six transistors is varied at a time.



$$\Delta M \cong u = \sum_i a_i x_i,\ \sigma_M^2 \cong \sum_i a_i^2 \sigma_i^2$$

$$\Delta I \cong v = \sum_i b_i x_i,\ \sigma_I^2 \cong \sum_i b_i^2 \sigma_i^2$$

x_i : ΔV_{TH} of a transistor

Fig.4 Linear approximation is applied to a parameter space of interest.

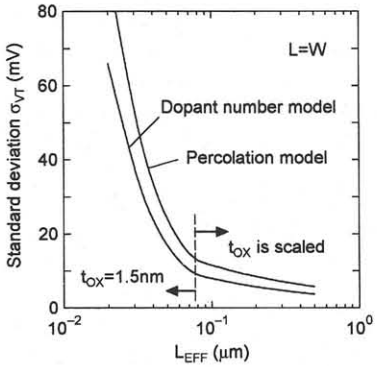


Fig.5 Dopant-induced V_{TH} fluctuation predicted by existing models.

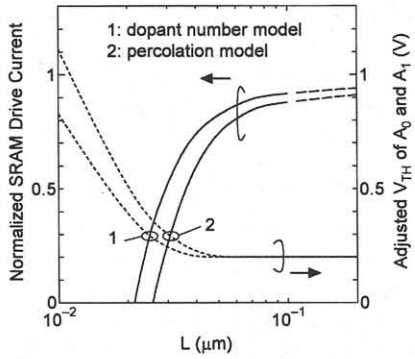


Fig.6 Worst case SRAM read current (normalized by center value) vs L for bulk CMOS.

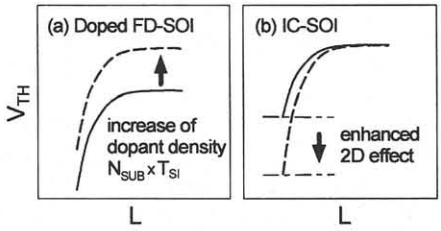
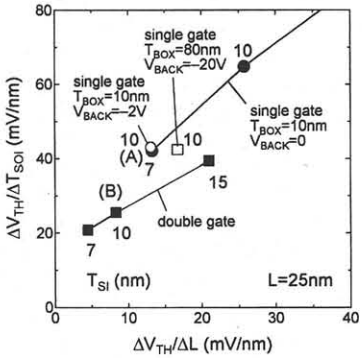


Fig.7 Typical dependence of V_{TH} on T_{SI}.



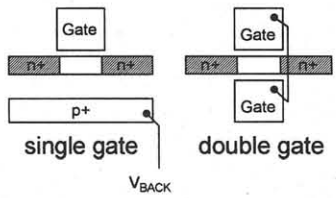


Fig.8 $\Delta V_{TH}/\Delta T_{SI}$ vs $\Delta V_{TH}/\Delta L$ for 25nm SOI FETs for various structures and V_{BACK}. Data points (A) and (B) are used in the text.

	(A) planer single gate	(B) vertical double gate
K_T (mV/nm)	43	25
K_L (mV/nm)	13	8.3
$K_T \Delta T_{SI}$ (mV)	43	63
$K_L \Delta L$ (mV)	33	21
ΔV_{TH} (mV)	76	83

Table 1 Estimation of IC-SOI V_{TH} variation. (A) ΔT_{SI}=±1nm, (B) ΔT_{SI}=±2.5nm.

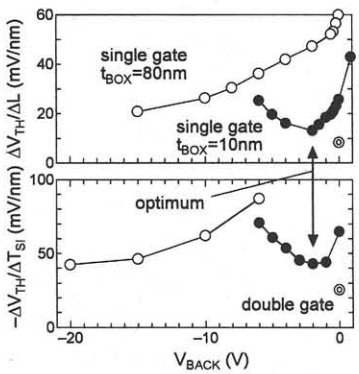


Fig.9 $\Delta V_{TH}/\Delta T_{SI}$ and $\Delta V_{TH}/\Delta L$ vs back bias. Optimum V_{BACK} exists for single gate SOI, where vertical field is minimized without forming a back channel.

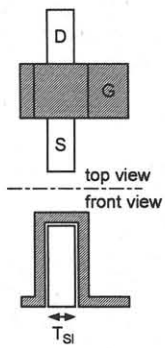


Fig.10 Vertical double gate SOI.

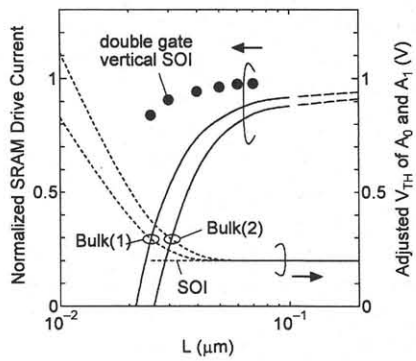


Fig.11 Worst case SRAM read current for vertical double gate SOI CMOS. Results for bulk in Fig.5 is also shown for comparison.

References

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