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# Impact of Strained-Si Channel on CMOS Circuit Performance under the Sub-100nm Regime

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## 1. Introduction

Recent experiments and theoretical calculations show that the electron and hole mobilities in strained Si layers pseudomorphically grown on relaxed $Si_{1-x}Ge_x$ are significantly enhanced [1,2,3,4]. Thus, strained-Si MOSFETs, schematically shown in Fig.1, are regarded as one of the promising device structures in sub-100nm CMOS technology. However, benefits of the strained-Si MOSFETs with increased mobilities for sub-100nm CMOS circuits are not obvious, because the drive current of short channel MOSFETs is limited by the velocity saturation effect. On the other hand, the velocity overshoot effect is expected to relax the limitation due to the saturation velocity under sub-100nm gate-length MOSFETs. Consequently, quantitative circuit analysis, including clarification of detailed carrier transport properties of strained-Si, is strongly required in order to evaluate the impact of strained-Si MOSFETs on sub-100 nm CMOS technologies.

In this work, we investigate the effect of the enhanced mobility of strained-Si channel on the performance of sub-100nm CMOS circuits by the combined device and circuit simulation, considering both velocity saturation and velocity overshoot effects. It is found that higher mobilities of strained Si become more advantageous with reducing the channel length. It is also pointed out, for the first time, that the increase in energy relaxation time in strained Si, in addition to higher mobility, is effective for the enhancement of circuit performance.

## 2. Calculation Methods

Table 1 shows the structural parameters of strained-Si MOSFETs used as the input data of the device simulation. Fig.2 shows the mobility enhancement as a function of strain [3,4], which we have assumed in this study. Energy transport model (ETM), where the velocity saturation and velocity overshoot effects are modeled as the temperature-dependent mobility and local carrier heating, is used in the device simulation. The strain-dependent energy relaxation times, $\tau_w$, for electrons and holes, as a function of carrier temperature, are used in order to accurately describe the overshoot effect in strained-Si layers. Fig.3 shows the values of $\tau_w$ as a function of carrier temperature for bulk-Si and strained-Si [5]. In order to evaluate the effect of velocity overshoot on the drive current, I-V characteristics by Drift Diffusion Model (DDM) have also been simulated.

Parameters of a built-in MOSFET model in SPICE are extracted from the simulated results of I-V characteristics for strained-Si MOSFETs. The performance factor of CMOS circuits, which is inversely proportional to the propagation delay, is calculated from the oscillation frequency of 12-stage ring oscillators in SPICE simulation.

## 3. Results and Discussion

$I_{ON}$ enhancement as a function of mobility, $\mu$, and $\tau_w$ is shown in Fig. 4 and 5, respectively. It is found that, even in the ultra-short channel regime, $I_{ON}$ increases with an increase in $\tau_w$ as well as with an increase in $\mu$, because of the enhancement of the velocity overshoot effect. The strong $\tau_w$ dependence indicates the importance of considering the strain dependence of $\tau_w$. Fig.6 shows the $I_{ON}$ enhancement in strained-Si n- and p-MOSFETs. It is found that the significant increase in drive current due to strain is obtained for both n- and p-MOSFETs. It is also found from the comparison of the calculated results between ETM and DDM that half of the $I_{ON}$ enhancement in p-MOSFETs and 3/4 of that in n-MOSFETs is attributable to the velocity overshoot effect.

Fig.7 shows the relative performance factor of strained-Si CMOS against bulk-Si CMOS. The performance enhancement of strained-Si CMOS on a $Si_{0.7}Ge_{0.3}$ substrate is found to reach 65%, which corresponds to that accomplished by device scaling of bulk-Si CMOS technology over about 2 generations. Fig.7 also shows that half of the performance enhancement originates in the increase in $\tau_w$ due to strain. It is found, as a result, that the increase in $\tau_w$ due to strain makes strained-Si CMOS more advantageous in the ultra-short channel regime.

Fig.8 shows the performance factor enhancement of the strained-Si CMOS on a $Si_{0.7}Ge_{0.3}$ substrate as a function of gate length, $L_G$. It is found that the circuit performance enhancement of strained-Si CMOS to bulk-Si CMOS increases with reducing $L_G$, because of the enhancement of the velocity overshoot effect. Fig.9 shows the comparison of the performance enhancement between bulk- and strained-Si CMOS normalized by the performance of bulk Si at $L_G$ of 100nm. It is confirmed that the performance enhancement by device scaling under the sub-100nm regime is much larger in strained Si than in bulk Si.

## 4. Conclusion

The performance enhancement of strained-Si CMOS circuits under the sub-100nm regime was quantitatively evaluated. It was found that the enhancement of velocity overshoot due to strain increases the circuit performance by around 2 generations of device scaling.

## References

[1] J. Welser, et al., IEEE IEDM Tech. Dig., p. 373(1994) [2] K. Rim, et al., IEEE IEDM Tech. Dig., p. 517(1995) [3] S. Takagi, et al., J. Appl. Phys., **80**, 1567 (1996) [4] R. Oberhuber, et al., Phys. Rev. B, **58**, 9948(1998) [5] F. M. Bufler, "Full-Band Monte Carlo Simulation of Electrons and Holes in Strained Si and SiGe", Herbert Utz Verlag, München, 1998

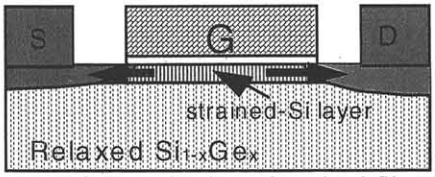


Fig.1 Schematic view of strained-Si MOSFET

| | Lg=50nm(Leff=35nm) | | Lg=100nm(Leff=70nm) | |
|---|---|---|---|---|
| | PMOSFET | NMOSFET | PMOSFET | NMOSFET |
| Tox(nm) | 2.1 | 2 | 3.6 | 3.5 |
| Cj(nm) | 10 | 10 | 20 | 20 |
| Ns(cm-3) | $1.2\times10^{18}$ | $1.3\times10^{18}$ | $7\times10^{18}$ | $7.3\times10^{18}$ |
| Vth(V) | -0.3 | 0.3 | -0.4 | 0.4 |
| Vdd | 0.9 | | 1.5 | |

Table1 Structural parameters of strained-Si MOSFETs as the input data of the device simulation

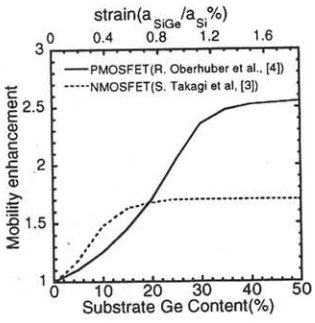


Fig.2 Mobility enhancement of a strained-Si MOSFET as a function of strain

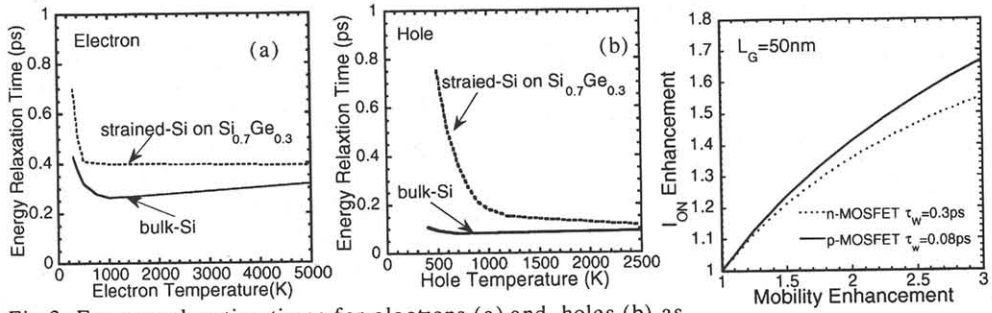


Fig.3 Energy relaxation times for electrons (a) and holes (b) as a function of temperature in strained-Si and bulk-Si

Fig.4 $I_{ON}$ ($I_D$@ $V_D=V_{DD}$, $V_g=V_{DD}$) enhancement of strained-Si MOSFETs as a function of mobility enhancement, where energy relaxation time is kept constant

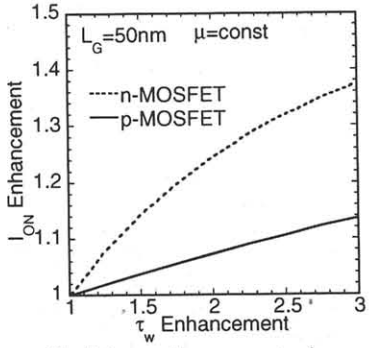


Fig.5 $I_{ON}$ enhancement of strained-Si MOSFETs as a function of energy relaxation time enhancement, where the mobility is kept constant

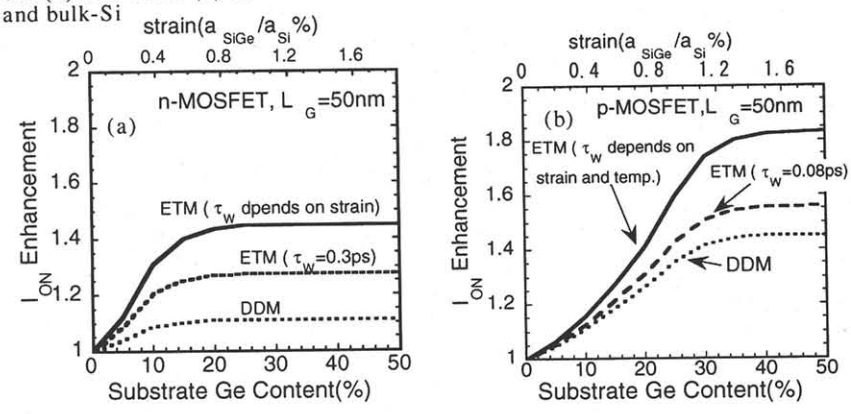


Fig. 6 $I_{ON}$ enhancement of strained-Si n-MOSFET(a) and p-MOSFET(b) as a function of a substrate Ge content, or strain of channel, where mobility and tware enhanced according to Fig. 2 and Fig. 3(line), mobility is enhanced (broken line) but tw is not enhanced, and mobility is enhanced but velocity overshoot is not considered (dot line, calculated results by DDM)

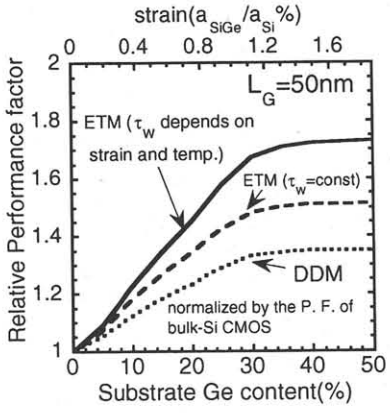


Fig. 7 Relative performance factor enhancement of strained-Si CMOS as a function of a substrate Ge content where mobility and energy relaxation time are enhanced according to Fig.2 and Fig3(line), mobility is only enhanced (broken line), and mobility is enhanced but velocity overshoot is not considered (dot line)

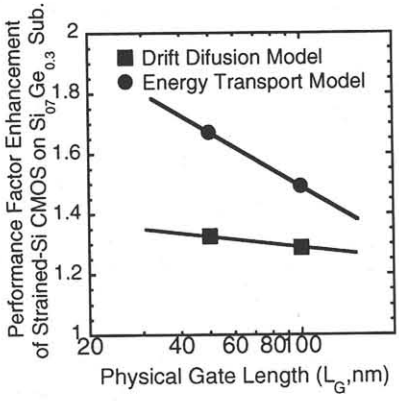


Fig. 8 Performance factor enhancement of strained-Si CMOS on a $Si_{0.7}Ge_{0.3}$ substrate as a function of gate length, where performance factors are normalized by that of bulk-Si CMOS with the same gate length

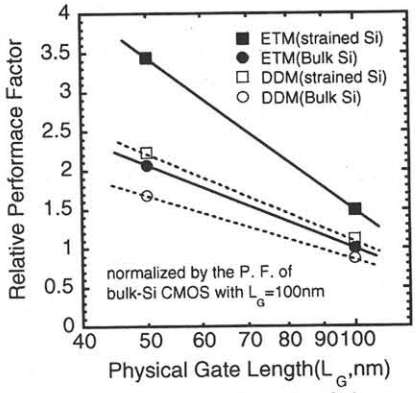


Fig. 9 Performance factors of the strained-Si CMOS on a $Si_{0.7}Ge_{0.3}$ substrate and bulk-Si CMOS as a function of gate length, where performance factors are normalized by that of bulk-Si CMOS with $L_G$=100nm