Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 64–65

B-2-5

Improved Low Temperature Characteristics of Raised Source and Drain (RSD) Si_{1-x} Ge_x PMOSFET's

H. J. Huang [a], K. M. Chen[a], T. Y. Huang[a], and G. W. Huang[b], C. Y. Chang[a]

[a]Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. Tel: 886-3-5726111ext31800, Fax: 886-3-5721500

[b]National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

Electronic mail: cyc@cc.nctu.edu.tw

Abstract—$Si_{1-x}Ge_x$ RSD PMOSFET's have been fabricated and are further studied for low temperature applications. The devices exhibits well short channel behavior and perfect leakage characteristics by using 100nm $Si_{1-x}Ge_x$ epitaxial layer on source and drain for its shallow junction and less implantation damage. Relative better output characteristics at 25°C and greater improvement in low temperature behavior (-50°C) were achieved and appealed as a potentially promising approach for MOSFET technology.

Introduction

Base on the demand for sub-0.1μm device, shallow junctions obtained by out-diffusion from in-situ doped or ion-implanted p^+/n^+ SiGe layer have been reported [1], [2]. $Si_{1-x}Ge_x$ is particularly suitable for such application, because it can be selectively deposited onto the exposed S/D areas. Furthermore, $Si_{1-x}Ge_x$ has lower Schottky barrier height with respect to p^+ junctions because of the reduced band gap, which is beneficial for achieving low contact resistivity [3], [4], [5]. Recently, PMOSFET's with using $Si_{1-x}Ge_x$ as S/D layer have been fabricated, and the its impacts on contact resistance and device performance have been demonstrated [5]. In this work, continuous research on DIBL improvement for $Si_{1-x}Ge_x$ RSD PMOSFET's and its temperature dependence on device performance were studied. The specific contact resistivity and sheet resistance variations as a function of time were also studied in detail.

Experiment

P-channel MOS transistors with raised source/drain structure were fabricated by standard process in the beginning. Following 4nm gate oxide and polysilicon gate formation, source/drain extension implant and a 800°C, 20 min furnace anneal accompany with RTA 1050°C, 10sec for activation was performed. After a 150 nm sidewall spacer formation, wafers were split to receive SiGe or Si selective epitaxial growth (SEG) on the exposed S/D regions by ANELVA SRE-612 cold-wall ultra-high vacuum chemical molecular epitaxy (UHVCVD) system. For comparison, conventional Si MOS transistors (i.e., without any raised S/D layer) were also fabricated in the same run. To obtain higher degree of boron concentration in S/D region, a 5E15 cm^{-2} BF_2 implant was adopted. The varied-temperature measurements were performed with HP4156 system in addition to a thermal controller connected to the Cascade semi-auto probe station with a range from -50°C to 100°C.

Results and Discussion

Fig.1 compares the I_D-V_G characteristics of $Si_{0.86}Ge_{0.14}$ RSD MOSFET and conventional Si one. It can be seen that the device with $Si_{0.86}Ge_{0.14}$ RSD produces Gm and I_D value (measured at V_D = -2.5 V and V_G - V_T= -1.8 V) of 127 mS/mm and 158.6 μA/μm, which are 19.02% and 16.11% more than that of conventional Si device respectively, both with the same effective channel length (e.g., 0.24 μm). This improvement is believed to be caused by the lowering of Schottky barrier height (SBH) in metal/$p^+Si_{1-x}Ge_x$ junction, which leads to the reduction of specific contact resistivity[6]. The relative contact resistivity measured by TLM method and resultant transconductance value as a function of Ge molefraction were given in Fig. 2. These improvements in device performance are more apparent with device scaling down.

With thicker epitaxial thickness on S/D region, shallower S/D p^+ junction could be obtained. Fig. 3 implied a better DIBL effect for RSD $Si_{1-x}Ge_x$ MOSFET with epitaxial thickness of 100nm. In addition, for 100nm RSD MOSEFT's, the implantation damage could be lighter because the atom-injection region is away from the S/D p^+-n junction. The resultant lower leakage level could be proved in Fig. 4.

Fig. 5 and Fig. 6 demonstrate the subthreshold and transconductance characteristics of conventional Si and RSD $Si_{0.91}Ge_{0.09}$ PMOSFET's operated at various temperatures. Substantial changes in drain current could be obtained in Fig. 7. Generalized saturation transconductance Gm versus effective channel length in Fig. 8 reveals the superior room temperature and low-temperature performance for $Si_{0.86}Ge_{0.14}$ RSD MOSFET's. Normalized linear Gm value and saturation drive current at –50°C with respect to the same parameter at 100°C in Fig. 9 and Fig. 10 also indicate remarkable increase for RSD MOSFET's, as compared with conventional Si ones.

In order to observe the temperature variations in intrinsic and extrinsic part of MOS device, sheet resistance and contact resistance (measured by CBKR method) as a function of temperature were illustrated in Fig. 11 and Fig. 12. Sheet resistance and channel resistance decreases as reducing temperature due to enhancement of mobility. On the contrary, specific contact resistivity increases with reducing temperature because of less carriers capable of overcoming the metal/semiconductor energy barrier, especially for conventional Si sample with higher energy barrier. We believed that the steeper slope and larger value as shown in Fig. 12 for Si sample, is the reason why its low temperature is not so impressive as RSD $Si_{1-x}Ge_x$ MOSFET's.

Conclusions

In this paper, raised source and drain (RSD) $Si_{1-x}Ge_x$ PMOSFET's were fabricated and measured for further DIBL and temperature dependence study. RSD $Si_{1-x}Ge_x$ MOSFET's demonstrate excellent electrical characteristics including better driving current and transconductance, better short channel effect behavior, smaller leakage current, superior low temperature characteristics. With overcome the epitaxial quality problem, these performance improvements make it a very attractive device structure for future sub-0.1μm salicided or nonsalicided p-channel MOS transistors.

References

[1] M.Ono, M.Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50 nm gate length n-MOSFET's with 10nm phosphorus source and drain junction." *IEDM Tech. Dig.*, pp. 119-122, 1993.

[2] J. Sakano and S. Furukawa, "Study of shallow p+n junction formation using SiGe/Si system," *Jpn. J. Appl. Phys.* Vol. 32, pp. 6163-6167, 1993.

[3] F. S. Johnson, D. S. Miles, D. T. Grider, and J. J. Wortman, "Selective chemical etching of polycrystalline SiGe alloys with respect to Si and SiO2," *J. Electron. Mater.*, vol. 21, no.8, pp. 805-810, 1992.

[4] V. Aubry, F. Meyer, P. Warren, and D. Dutartre, "Schottky barrier heights of W on $Si_{1-x}Ge_x$ alloys," *Appl. Phys. Lett.*, vol. 63, no. 18, pp. 2520-2522, 1993.

[5] H. J Huang, K. M Chen, C. Y Chang, L. P Chen, G. W Huang, and T. Y Huang, "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain", *submitted to Electron. Device Lett.*

[6] C. G. Van de Walle and R. Martin, *Phys. Rev.* B. vol.34, pp. 5621, 1986.

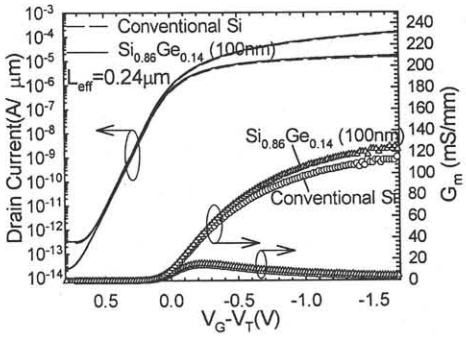

Fig 1. Subthreshold, transconductance and output characteristics of a conventional Si and a $Si_{0.86}Ge_{0.14}$ RSD MOSFET's with a gate oxide thickness of 4 nm.

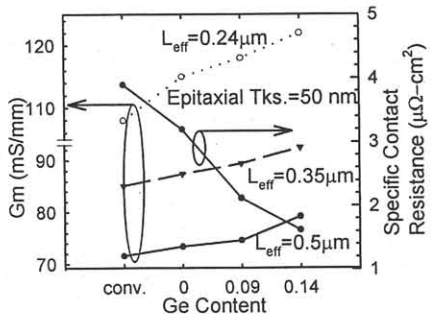

Fig. 2 Transconductance Gm as a function of Ge relative ratio in selective $Si_{1-x}Ge_x$ epitaxial layer with different effective channel length. The specifc contact resistivity as a function of Ge molefraction is also demonstrated in this figure.

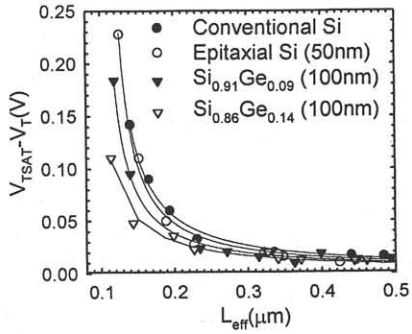

Fig. 3 DIBL(V_{TSAT}-V_{TLIN}) for PMOS transistors with different S/D structure.

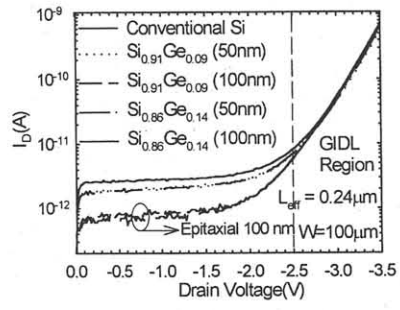

Fig. 4 Measured drain leakage I current as a function of drain bias in off-state(V=0V) for conventional Si and RSD SiGe PMOS transistors.

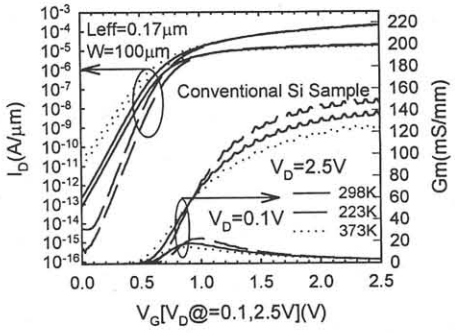

Fig. 5 Subthreshold characteristics and transconductance of conventional Si PMOS transistor measured at various temperatures.

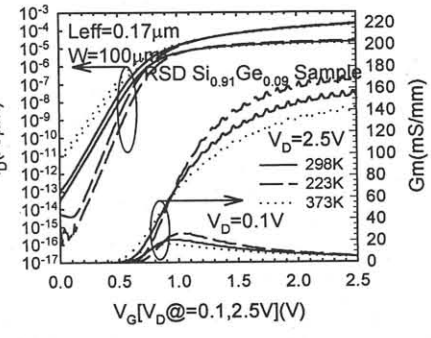

Fig. 6 Subthreshold characteristics and transconductance of RSD $Si_{0.91}Ge_{0.09}$ PMOS transistor measured at various temperatures. The epitaxial thickness is 100 nm.

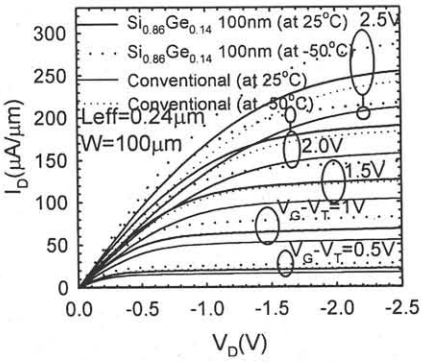

Fig. 7 Measured Drain current versus drain voltage of conventional Si and RSD $Si_{0.86}Ge_{0.14}$ PMOS transistors.

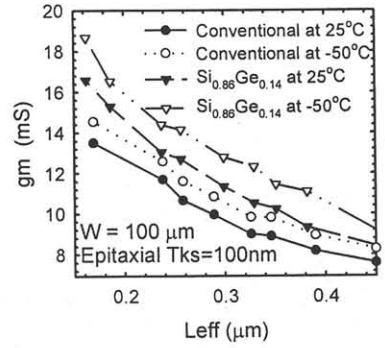

Fig. 8 Saturated transconductance, Gm versus effective gate length measured at various temperature for conventional Si and RSD $Si_{0.86}Ge_{0.14}$ sample.

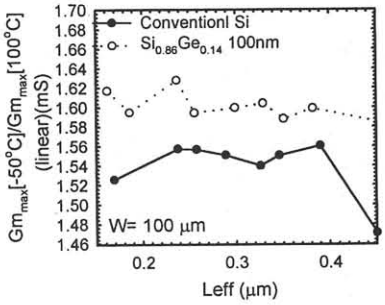

Fig. 9 The normalized value, Gm_{max}[-50°C]/Gm_{max}[100°C] versus effective gate length for conventional Si and RSD Si0.86Ge0.14 sample.

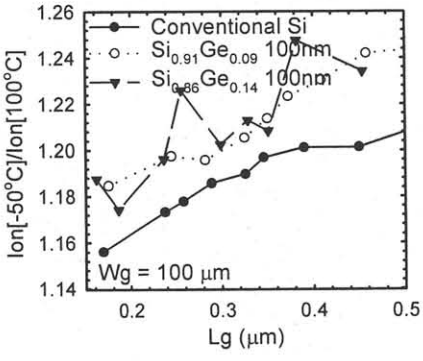

Fig. 10 The normalized value, Ion[-50°C]/Ion[100°C] versus effective gate length for conventional Si and RSD $Si_{0.91}Ge_{0.09}$, and $Si_{0.86}Ge_{0.14}$ sample.

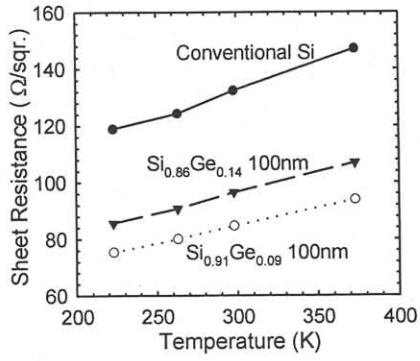

Fig. 11 Sheet resistance value as a function of temperature for diffusion region with different structure.

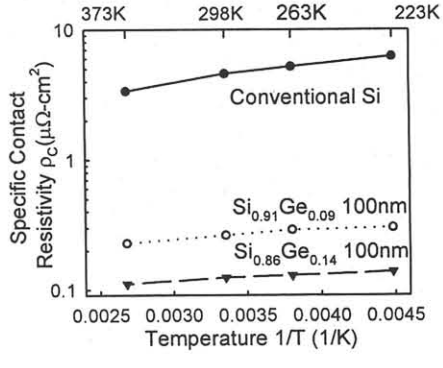

Fig. 12 Specific contact resistivity ρ_C as a fuction of reciprocal temperature (1/T) for metal with different contact layer structure.