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Edge Direct Tunneling (EDT) Induced Drain and Gate Leakage in Ultrathin Gate Oxide MOSFETs

K. N. Yang, H. T. Huang, M. J. Chen
Department of Electronics Engineering, National Chiao-Tung University
Hsin-Chu, Taiwan, ROC
Tel: +886-3-5712121ext54217 e-mail: mjchen@RPL.ee.nctu.edu.tw

Y. M. Lin, M. H. Yu, S. M. Jang, C. H. Yu, M. S. Liang
R/D Department, Taiwan Semiconductor Manufacturing Company
Hsin-Chu, Taiwan, ROC
Tel: +886-3-5781688ext3586

1. Introduction

The off-state drain leakage is one of the big issues for aggressively shrunk MOSFETs. The well recognized mechanisms are the gate-induced-drain-leakage(GIDL) [1],[2], the bulk band-to-band tunneling(BTBT) [3], and the DIBL(drain induced barrier lowering) enhanced subthreshold conduction. In the case of reverse substrate bias for suppression of DIBL and thereby subthreshold leakage, the bulk BTBT dominates [4]. On the other hand, the gate leakage due to direct tunneling was measured *per unit oxide area* and a certain criterion of 1 A/cm^2 set the ultimate limit of scalable oxide thicknesses [5],[6]. In this paper, we report that as scaled gate oxide thickness approaches the direct tunneling regime, the edge direct tunneling(EDT) of electrons from n$^+$ polysilicon to underlying n-type drain not only dominates the gate leakage, but also can prevail over the conventional GIDL and bulk BTBT. This phenomenon is more pronounced for thinner oxide thicknesses, and EDT can even compete over the bulk BTBT in the case of reverse substrate bias. In particular, it is clarified that the gate leakage *in stand-by mode* indeed originates from the edge part rather than the whole gate oxide, and thus should be measured *per unit gate width* rather than per unit oxide area as in [5],[6].

2. Experiment and Characterization

The n$^+$ poly-gate nMOSFETs were fabricated by a 0.18-um process technology [7]. The gate oxides were grown in diluted wet oxygen ambient to three different thicknesses T_{ox} of 1.47, 2.15, and 2.40 nm. These oxide thicknesses were determined by an electron direct tunneling I-V model [8]. Fig. 1 shows experimental and calculated gate current versus oxide field for gate injection through the whole oxide to underlying bulk. The corresponding oxide field, also serving as input parameter to the model, was obtained in advance by employing a C-V integration technique [9]. These extracted oxide thicknesses were confirmed by both high resolution TEM and C-V method accounting for polysilicon depletion and Quantum Mechanical effects.

Fig. 2 illustrates the tunneling leakage paths and related band diagrams. With source open and under $V_G = -V_D$, the measured drain current I_D, gate current I_G, and bulk current I_B are plotted in Fig. 3 versus V_{DG} for three different oxide thicknesses. Fig. 3 reveals that the drain current primarily comprises the GIDL, the bulk BTBT, and the gate current, implying the EDT as the origin of the latter component. It can be observed that the EDT dominates the gate leakage, and there exists a certain range where the EDT prevails over the conventional GIDL and bulk BTBT. This phenomenon is more pronounced for thinner oxide thicknesses. In Fig. 3(c) for 1.47 nm thick oxide, the polarity of the bulk current is reversed due to gate-to-bulk tunneling.

With source grounded and V_D =1 V, the measured terminal currents versus both polarities of V_G are plotted in Fig. 4 for substrate bias V_B = 0 and –1 V. Obviously, for T_{ox} = 2.40 nm the bulk BTBT at V_B = -1V dominates the drain leakage in –0.5V $<V_G<$0V, while such role is replaced by EDT for thinner oxides. In Fig. 4(b) and (c), the $I_D(\cong I_G)$ for V_G < 0V seems to be unchanged with and without substrate bias, supporting the EDT mechanism responsible. Besides, we found experimentally that the EDT leakage is indeed proportional to the gate width, regardless of the aspect ratio(W/L). This means that the gate leakage in stand-by mode(i.e., only source and gate tied to ground) should be adequately measured per unit gate width.

3. EDT Modeling

An analytic electron direct tunneling model [8] was employed. The oxide field E_{ox} at the gate edge is one key input parameter to the model, and can be obtained by solving the following equation:

$$V_{DG} - V_{FB}(\cong 0) = V_{poly} + T_{ox}E_{ox} + V_{LDD} \qquad (1)$$

Applying the first subband approximation to the accumulated n$^+$ poly gate and the deep depletion approximation to the underlying LDD region as shown in Fig. 5, we get

$$(E_f - E_1)\frac{q\eta m_d}{\pi\hbar^2} = \varepsilon_{ox} E_{ox}, \quad E_1 = \frac{(3\pi\hbar q\, m_{si,\perp})^{2/3}}{2\, m_{si,\perp}}\left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} E_{ox}\right)^{2/3}$$

$$V_{poly} \cong E_f/q = \varepsilon_{ox}E_{ox}\frac{\pi\hbar^2}{\eta m_d q^2} + E_1/q, \quad V_{LDD} = \frac{\varepsilon_{ox}^2 E_{ox}^2}{2q\varepsilon_{si} N_{LDD}}$$

Here $m_{Si,\perp}$=0.32 m_o, $m_{Si,\parallel}$=0.25 m_o and η=4 to approximate the band-structure for <110> oriented n+-polysilicon grains [8]. (1) can further be rearranged as:

$$V_{DG} \cong a_1 E_{ox} + a_2 E_{ox}^2 + a_3 E_{ox}^{2/3} \qquad (2)$$

where

$$a_1 = T_{ox} + \frac{\pi\hbar^2}{\eta m_d q^2}\varepsilon_{ox}, \; a_2 = \frac{\varepsilon_{ox}^2}{2q\varepsilon_{Si} N_{LDD}}, \; a_3 = \frac{(3\pi\hbar q\, m_{Si,\perp})^{2/3}}{2\, q\, m_{Si,\perp}}\left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right)^{2/3}$$

Thus, it is easy to extract E_{ox} by solving (2) numerically. The effective edge-tunneling area $A_o(=L_T \times W)$ can be extracted based on the model [8]:

$$I_{EDT} = A_o Q f T = L_T W Q f T \qquad (3)$$

where Q is sheet charge of the accumulation layer, f is electron impact frequency on the n$^+$-poly/SiO_2 interface and T is the modified transmission probability considering interface reflection factor. Once E_{ox} was quantified, an excellent reproduction was achieved with $N_{LDD}=3\times10^{19}$ 1/cm^3 and effective mass m_{oxe} =0.61 m_o resulting from Franz-type dispersion relation in tunneling oxide, as depicted in Fig. 6. The tunneling path extracted was 0.00625 um wide(=L_T) from the gate edge(due to N_{LDD} extracted). This is quite reasonable since the drain extension beneath the gate is about 0.01 um. Therefore, the consistent modeling work validates the EDT as the origin of the leakage of concern.

4. Conclusion

The edge direct tunneling(EDT) of electrons from n$^+$ polysilicon to underlying n-type drain has shown its tremendous impact on the drain leakage and gate leakage. This effect is more pronounced for thinner oxide thicknesses. It is clarified that the gate leakage in practical stand-by mode should be measured per unit gate width, particularly for MOSFETs with oxide thickness less than 2.40 nm. Eventually, a physical model cited in the literature does reproduce consistently experimental EDT I-V characteristics and its tunneling area extracted indeed falls within the gate-to-drain overlap region.

Acknowledgment

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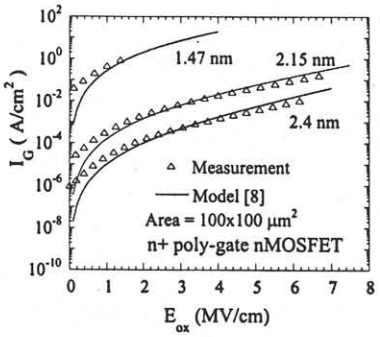

Fig. 1 D-T(Direct-Tunneling) technique for the oxide thickness determination.

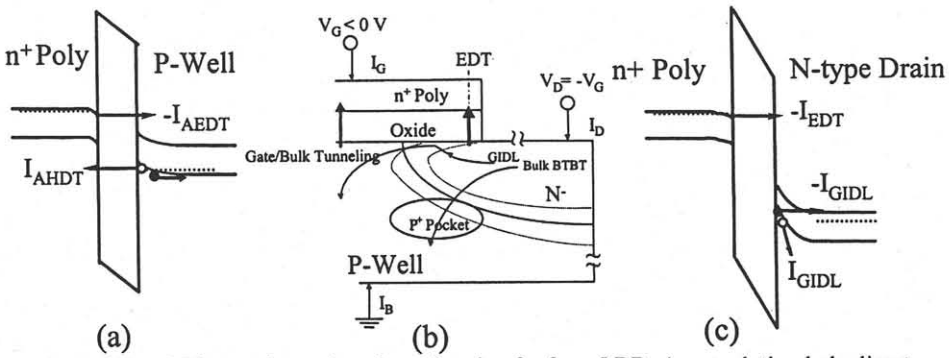

Fig. 2 (a)Band Diagram located at channel region far from LDD. Accumulation hole direct tunneling current (I_{AHDT}) and accumulation electron direct tunneling(I_{AEDT}) both contribute to Gate-to-Bulk tunneling current. (b) Schematic cross-section near gate/drain overlap region under $V_G<0$ V and $V_D= -V_G$. Different tunneling paths are shown. (c) Band Diagram located at gate/drain overlap region, showing EDT and GIDL under off-state condition.

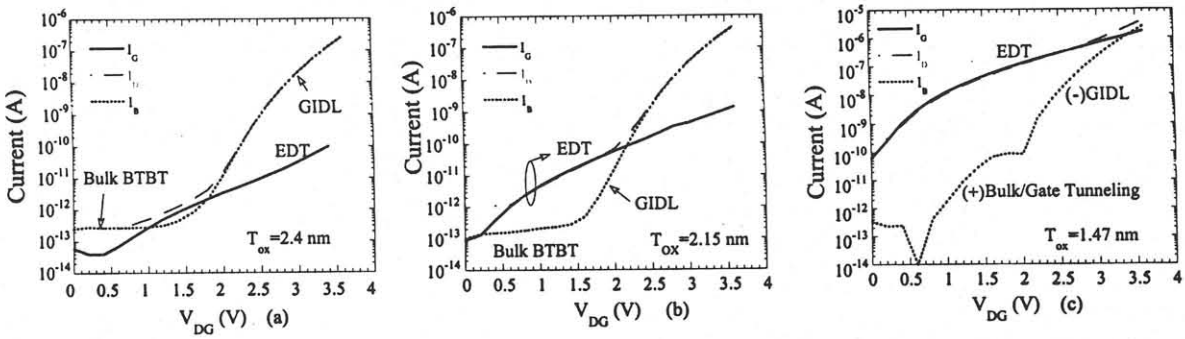

Fig. 3 Displaying the measured terminal currents versus V_{DG} for three different T_{ox} (a), (b), and (c) under $V_G= -V_D$ and source open. The aspect ratio W/L=10 μm / 0.5 μm. (a) EDT dominates the drain leakage in 1 V<V_{DG}<1.8 V. (b) The edge tunneling mechanism dominates I_D for 0 V<V_{DG}< 2.2 V, and GIDL constitutes drain leakage for V_{DG}>2.2 V. (c) The edge tunneling mechanism prevails over almost the drain leakage current. Note that Gate-to-Bulk tunneling is an important leakage source for I_B in 0.5 V<V_{DG}<2 V.

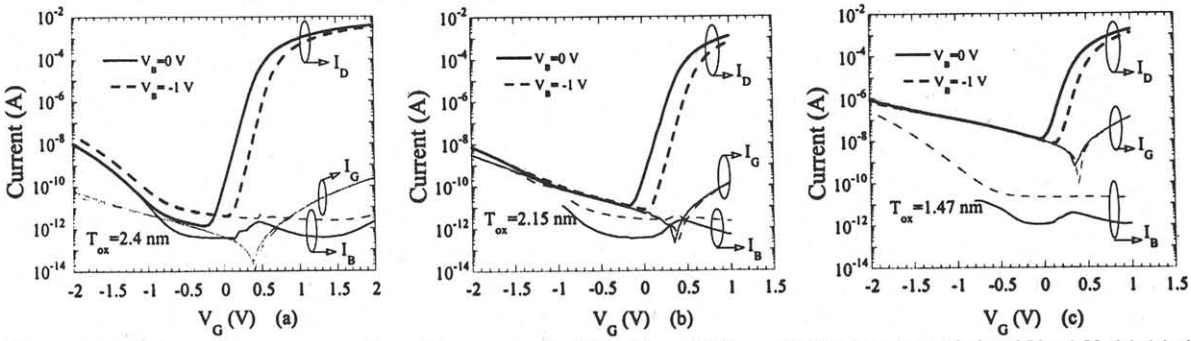

Fig. 4 Measured terminal current versus gate voltage. The aspect ratio W/L=10 μm / 0.5 μm. With source grounded and V_D=1 V, (a)-(c) show the measured terminal currents versus both polarities of V_G for substrate bias V_B=0 and -1 V. (b) and (c) exhibit that off-state drain current does not come from GIDL or bulk BTBT but EDT due to the evidence, $I_G \cong I_D$.

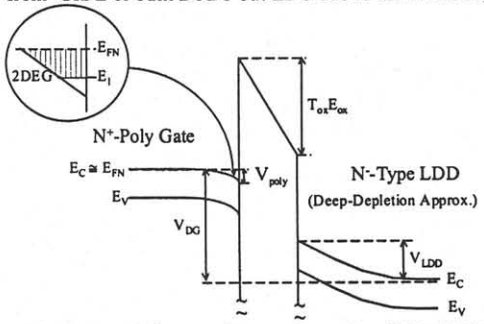

Fig. 5 Band diagram drawn along Gate/SiO_2/LDD. The accumulation potential bending, V_{poly}, with 2DEG concept and the silicon surface potential bending, V_{LDD}, with the deep depletion approximation are adopted in the procedure of E_{ox} extraction.

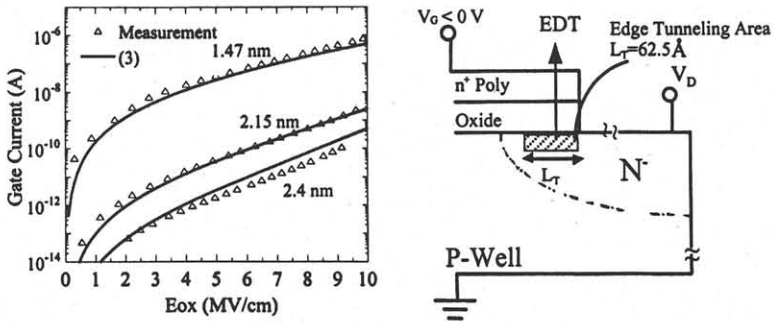

Fig. 6 Comparison of the EDT calculation and experiment. The extracted effective EDT range is 62.5 Å wide from the gate edge, equal for three different oxide thickness. W=10 μm.