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Modeling of the Series Resistance for Below 100nm MOSFET Regime

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I. Introduction

As the Si-MOSFET's are scaled down, there is increasing concern about series resistance that may limit the ultimate performance [1]. In order to minimize the series resistance and optimize the source/drain structure, it is necessary to understand the relative contribution of the device and process parameters on the total series resistance and select the appropriate process and device parameter such as implantation dose and energy, temperature budget, sidewall thickness and salicide thickness. There are many papers on the modeling of the series resistance. However, most of them did not consider the extremely short channel structure [2].

In this work, we have developed an accurate new model that can describes a shallower SDE junction structure with higher doping concentration, relatively enlarged sidewall length, silicide-diffusion contact system, and high-κ dielectric sidewall. With the proposed model, we can analyze the impact of the device parameters on the series resistance as well as accurate resistance estimation.

II. Modeling

The current density contours using SILVACO simulation tools show the depletion width in the SDE junction is relatively enlarged owing to shallower junction depth in deep submicron MOSFET and the surface channel current flows through the accumulation layer spreads out into the SDE and deep junction region along the depletion region boundary (Fig. 1). The series resistance can be divided into the four components. Overlap resistance (R_{ov}); extension resistance (R_{ext}); deep resistance (R_{dp}); and silicide-diffusion contact resistance (R_{cosd}). Each resistance component consists of the parallel or series combinations of sub-resistance components according to the carrier conduction path (Fig.2 (a) and (b)). In the regime below 100nm channel length, the doping concentrations in the SDE and deep region are relatively higher (between 10^{18} cm^{-3} and 10^{21} cm^{-3}). Therfore, the general empirical bulk mobility that covers for whole doping range was used in the modeling [3].

Since the current spreading takes place due to the unavoidable doping gradient and increased conduction paths, the doping gradient is very important for accurate calculation in the gate to SDE overlap region. Most of the resistance modeling assume the doping profile of the overlap region as a exponential function for simplicity [2]. However, the exponential doping profile is applicable only near the vicinity of the metallurgical junction, and it may produce significant errors far away from the junction.

In our model, Gaussian doping gradient is assumed in the overlap region where current accumulation and spreading occur. The overlap resistance is modeled by the series and parallel combination of R_{ac1}, R_{ac2}, and $R_{sp,ov}$ (Fig. 2). The current spreading starts at the end of the depletion region, W_{ext}. as can be seen in the simulation (Fig. 1). The depletion region widths, W_{ov}, W_{ext}, and W_{dp} can be found from the iterative solution with the simplified expression of the diffusion profile having exponential slope that is governed only near the vicinity of the junction. They also determine the current spreading angles. The surface region of the extension and deep region can be modulated by the fringing field from the gate edge, which would be effective for the deep submicron device with use of the high-κ dielectric sidewall. In this model, fringing resistances in the extension and deep region is derived with fringing capacitance which is obtained through conformal transformation [4]. The surface resistance in the extension region is easily obtained assuming uniform doping concentration within the projection range. The spreading resistance in the extension region can be modeled by vertical graded Gaussian doping profile and spreading angle α_2. The model considered the lateral encroachment of silicide in the deep region, since it could not be ignored as silicide thickness ($T_{silicide}$) increases in the deep submicron MOSFET with shallower junction. Also, the current in the deep region is assumed to spread with the identical spreading angle as in the case of the extension region. This assumption is conformed by 2-D simulation (Fig. 1). The silicide-diffusion contact resistance, R_{cosd} is defined as the resistance between the silicide contact and the diffusion layer underneath the silicide layer. It strongly depends on silicide thickness and the doping concentration of deep junction region, because the specific contact resistivity is determined by the active dopant concentration at the Si/Silicide interface. The model includes these effects with vertical Gaussian doping profile.

III. Implementation in below 100nm MOSFET

In order to verify and calibrate the proposed model, the process and device simulations were performed for various NMOSFETs with < 100 nm channel length. The input and output device parameters are shown in Table 1. The modeling results of total source series resistances with gate biases are in good agreement with simulation results except for the low gate bias (Fig. 3). The higher resistance of the simulation in low gate bias may be attributed to the appearance of a potential barrier in the overlap region due to the weak accumulation. The accumulation and spreading resistances in the overlap region are sensitive to the gate bias. R_{ac1} and R_{ac2} are decreases with gate biases as expected, while $R_{sp,ov}$ is slightly increases due to the decrease of the channel thickness, T_c (Fig. 4).

The proposed model can explain the relative contributions of each resistance components to the total series resistance as device is scaled down.(Fig. 5) It can be clearly seen from Fig. 5 that the silicide-diffusion contact resistance becomes dominant component which determines the total series resistance for future technology. From the sensitivity analysis of series resistance for the process parameters resulted from the proposed model, the small variations of the sidewall length and maximum doping concentration in the deep junction region considerably affect the series resistance variation (Fig. 6).

IV. Conclusion

A new model to calculate series resistance component accurately in the deep submicron MOSFET is presented. The model considers Gaussian diffusion profiles to minimize discrepancy with real profiles and current spreading angles changed by depletion width variations and is well suited for analyzing the characteristics of below 100nm MOSFETs such as the shallow junction, heavily doped SDE and deep region, silicide-diffusion contact, and high-κ sidewall material. The modeling results indicate that silicide-diffusion contact resistance may be a major resistance component for future technology and the sidewall thickness and the doping concentration in the deep junction region are the most sensitive process parameters.

V. References

[1] Y. Taur, et.al, *IEDM Technical Digest*, (1998) p. 789.
[2] K.K. Ng, et.al, *IEEE T-ED*, vol.33, no.7, (1986) p. 965.
[3] R.S. Muller, et.al, *John Wiley & Sons*, (1985) New York.
[4] S.S. Chung, et.al, *IEEE T-ED*, vol.39, no.3, (1992) p.614.

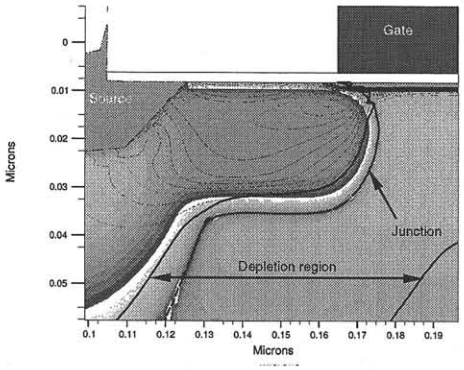

Fig. 1 The contours of current density on the triode region of 70nm NMOSFET where the contour of minimum current density is nearly zero and the increment is 1×10^5 A/cm^2.

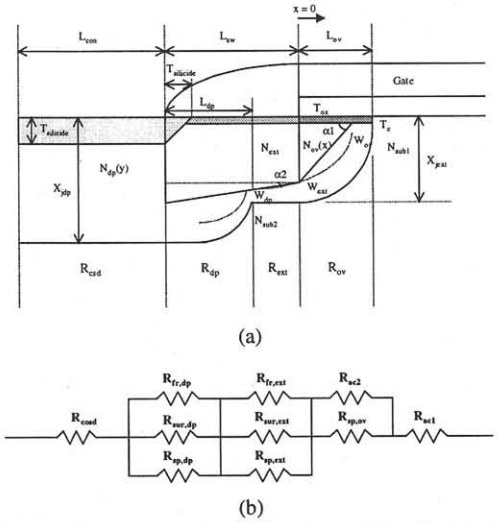

Fig. 2 (a) schematic representation for use in modeling of series resistance structure and (b) a equivalent circuits.

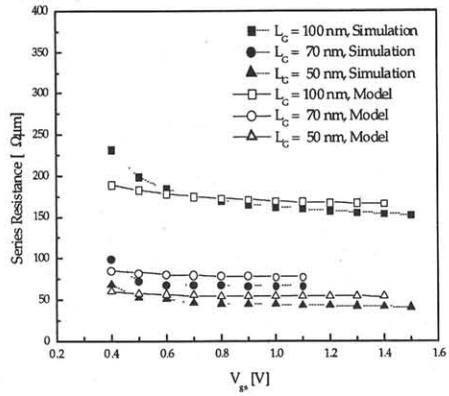

Fig. 3 Comparison of the series resistances with gate biases between proposed model and simulation results.

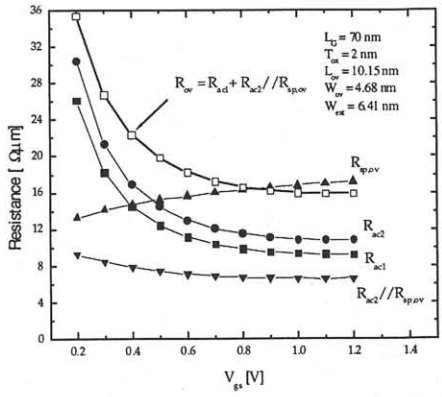

Fig. 4 Extracted resistance components of 70nm NMOSFET in the overlap region by using proposed model

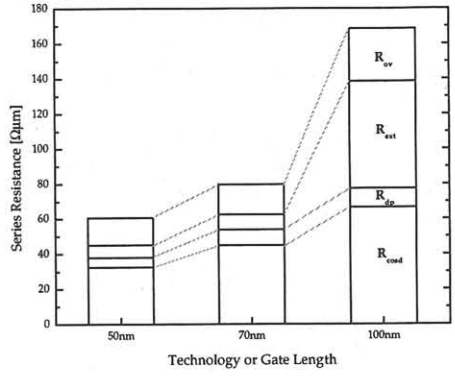

Fig. 5 Relative contributions of each resistance components to the total series resistance in below 100nm MOSFET regime calculated by proposed model.

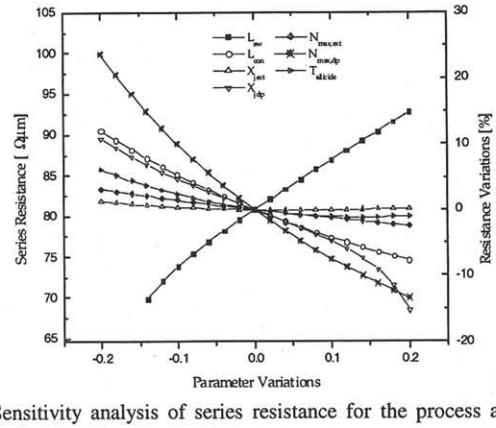

Fig. 6 Sensitivity analysis of series resistance for the process and device parameter.

Table 1. The Input device parameters used in this model and output parameters calculated from proposed model.

Input parameter / L_G	V_{DD} [V]	T_{ox} [nm]	L_{sw} [nm]	L_{ov} [nm]	L_{dp} [nm]	X_{jext} [nm]	X_{jdp} [nm]	$N_{max,ext}$ [cm^{-3}]	$N_{max,dp}$ [cm^{-3}]
50nm	0.5	1.5	40	9.0	32	26	66	4.0×10^{19}	3.2×10^{20}
70nm	0.7	2.0	60	10.2	49.7	29	70	3.5×10^{19}	2.8×10^{20}
100nm	1.0	2.0	100	20.0	55.1	32	94	5.0×10^{19}	1.8×10^{20}
Output parameter / L_G	T_C [nm]	N_{ac} [cm^{-3}]	α_1 [degree]	α_2 [degree]	W_{ov} [nm]	W_{ext} [nm]	W_{dp} [nm]	ρ_c [Ωcm^2]	
50nm	4.44	7.15×10^{12}	72.9	28.2	4.2	6.0	1.8	3.7×10^{-8}	
70nm	4.36	7.56×10^{12}	73.3	25.4	4.7	6.4	1.5	4.4×10^{-8}	
100nm	3.99	1.1×10^{13}	56.5	9.69	6.7	8.0	0.36	9.0×10^{-8}	