

Compact Expressions for Crosstalk of Multiple Bit Lines in DRAM

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1. Introduction

The crosstalk effect of two wires has been derived using distributed RC lines [1]. The extension for three wires including inductance effect has also been proposed [2]. However, for the DRAM arrays, inclusion of the more accurate model of MOSFET's instead of simple resistance significantly enhances accuracy. The model of a DRAM cell with one distributed RC bit line has been derived for the MOSFET in saturation [3] and triode regions [4]. Since the distance between the bit lines tends to shrink and the cell number on the bit line keeps increasing, accurate models of crosstalk help circuit designers design the sense amplifier and DRAM arrays. The compact expression combining accurate device models and distributed RC lines, as well as crosstalk of multiple bit lines for DRAM successfully predicts the waveforms on the bit line.

2. Compact Expressions

Fig. 1 shows the geometry of multiple bit lines coupled together and numbered from 2, 1, 0, 1 to 2 for any five consecutive bit lines. Each of them containing 2^x junction capacitors of cells are modeled as distributed RC lines. Before read operation, all the bit lines are precharged to $V_{dd}/2$. After the word line turns the even numbered cells on, the bit lines are charged or discharged. The sense amplifier is activated when the voltage difference between the even numbered bit line and the dummy bit line (odd numbered) reaches certain value.

In our previous work [4], the waveform model on a single bit line has been formulated using the following drain current equation, which is slightly modified from the current equation in saturation [5].

$$I_d = \frac{2W_{eff} \cdot C_{ox} \cdot v_{sat} \cdot (V_g - V_{t0} - (1 + \xi)V_s / 2 - \alpha V_d / 2)(V_d - V_s)}{\frac{2 \cdot v_{sat} \cdot L_{eff}}{\alpha} \left[1 + \left(\frac{V_g + V_{t0} - (1 - \xi)V_s}{\gamma \cdot T_{ox}} \right)^\beta \right] + (V_d - V_s)}$$

Where W_{eff} is the effective channel width; L_{eff} is the effective channel length; T_{ox} is gate oxide thickness; C_{ox} is the gate oxide capacitance per unit area. Other parameters are also modified to comply with the conditions of 0.35 μ m technology.

The derivation was performed for 5-coupled bit line. The voltage waveform (V_o) on a single bit line with distributed resistance R , capacitance C and length L can be obtained with the coupling capacitance of C_c between the bit lines.

$$V_o(x, t) = \frac{1}{5} V_{ini} \sum_{i=0}^2 \left\{ \left[1 + \sum_{k=1}^{\infty} A_{i,k}(x) \exp\left(\frac{-\delta_{i,k} t}{RC}\right) \right] \right. \\ \left. + \left[\left(2 - \frac{75-17\sqrt{5}}{24} i^2 + \frac{15-5\sqrt{5}}{24} i^4 \right) \left(A'_{i,0} + \sum_{k=1}^{\infty} A'_{i,k}(x) \exp\left(\frac{-\delta'_{i,k} t}{R(C + \frac{5-\sqrt{5}}{2} C_c)}\right) \right) \right] \right\} \\ \left. + \left[\left(2 - \frac{75+17\sqrt{5}}{24} i^2 + \frac{15+5\sqrt{5}}{24} i^4 \right) \left(A''_{i,0} + \sum_{k=1}^{\infty} A''_{i,k}(x) \exp\left(\frac{-\delta''_{i,k} t}{R(C + \frac{5+\sqrt{5}}{2} C_c)}\right) \right) \right] \right\}$$

$$\text{Where } \tan\left(\frac{\sqrt{\delta_{i,k}}}{\sqrt{\delta_{i,k}}}\right) = \frac{C_p \Gamma + C_L (\Gamma - C_p \delta_{i,k})}{(C_p \delta_{i,k} - \Gamma) + C_p C_L \Gamma \delta_{i,k}}, \text{ and} \\ A_{i,0} = \pm C_p / (1 + C_p + C_L)$$

$$A_{i,k}(x) = \pm \frac{2C_p \Gamma \left[\cos(x\sqrt{\delta_{i,k}}/L) - C_L \sqrt{\delta_{i,k}} \sin(x\sqrt{\delta_{i,k}}/L) \right]}{\left[P_1 \cos(\sqrt{\delta_{i,k}}) + P_2 \sin(\sqrt{\delta_{i,k}}) \right] / \sqrt{\delta_{i,k}}}$$

There are three normalization factors, $C + (5 - \sqrt{5})C_c / 2$, C , and $C + (5 + \sqrt{5})C_c / 2$, so C_L , C_c and C_p are C_b , C_c and C_p

normalized by different factors, and thus $\delta'_{i,k}$, $\delta''_{i,k}$, $A'_{i,k}$, and $A''_{i,k}$ are generated. Even though the solution is an infinite series, the first three exponential terms are accurate enough in the following evaluation.

3. Model Evaluation

To evaluate the accuracy of the new model, transient simulation of the structure with more than 10 bit lines in Fig. 1 was performed using SPICE with the BSIM3 model of 0.35 μ m with voltage on the gate=3.75V and the bit lines precharged to $V_{ini}=1.25V$. The capacitor C_p stores logic 1 and 0 with the voltages 2.5V and 0V, respectively. The nominal conditions are 256 cells on the bit line ($R=150\Omega$, $C=120fF$), 0.4 μ m between bit lines ($C_c=17.5fF$), $C_p=70fF$, and $C_f=80fF$. Fig. 2 demonstrates the agreement of V_o for the models marked "3-line" and "5-line" for 3-coupled and 5-coupled bit line models, respectively. The deviation is large if only one bit line labeled "single" is considered. In addition, for larger C_c , "3-line" model is not accurate enough. Figs. 3 and 4 plot the delay time when V_o reaching "(70% of ΔV) + V_{ini} " vs. the distance between the bit lines and the cell number on the bit line, where ΔV is the total voltage variation. When the distance reduces or the cell number increases, the delay time increases significantly and the voltage variation is reduced.

4. Conclusions

The compact expression for crosstalk of multiple bit lines in DRAM has been derived. The accuracy is very good for various conditions. The model with five coupled bit lines rather than three is important when the distance between the bit lines decreases.

References

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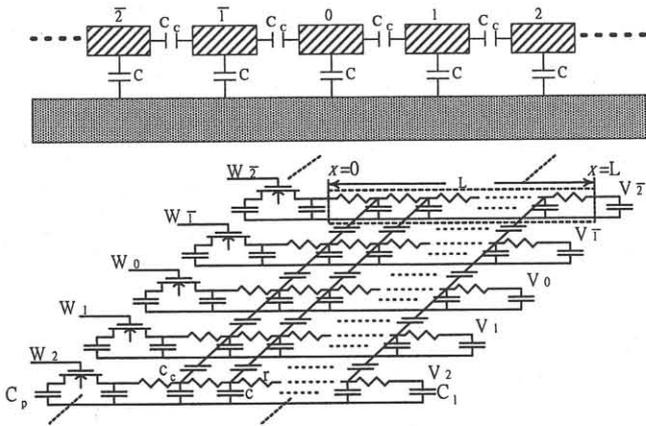


Fig. 1 The side view of the bit lines (top) and the equivalent circuit of DRAM arrays (bottom). For the following figures, “-” represents the dummy bit line.

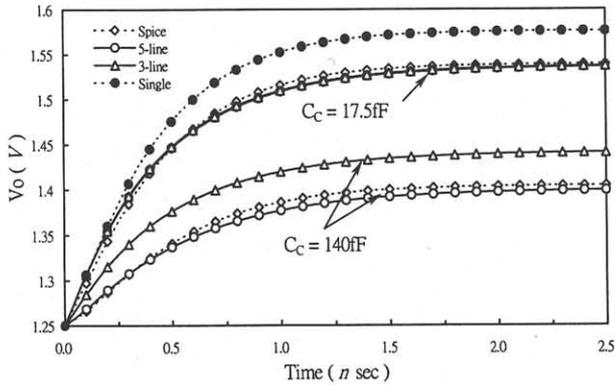


Fig. 2(a) The waveform of V_0 for read 1 in the array of ...0-0-1-0-0... with different C_c 's.

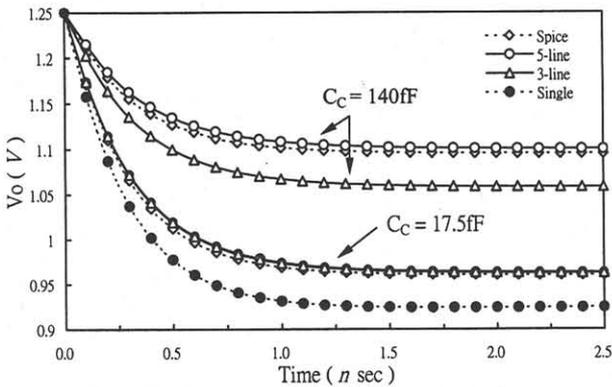


Fig. 2(b) The waveform of V_0 for read 0 in the array of ...1-1-0-1-1... with different C_c 's.

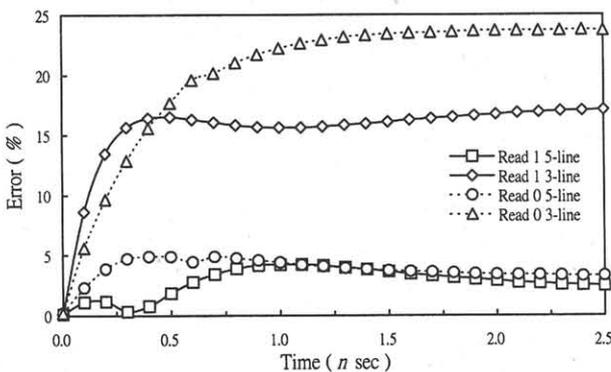


Fig. 2(c) The error is defined as the difference of V_0 between Spice and the model divided by the total variation from Spice for $C_c=140fF$.

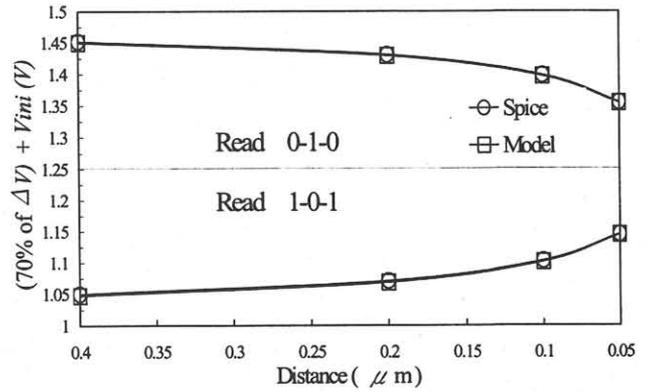


Fig. 3(a) V_0 reaching “(70% of ΔV) + V_{ini} ” using the 5-line model agrees with Spice for different distances between the bit lines.

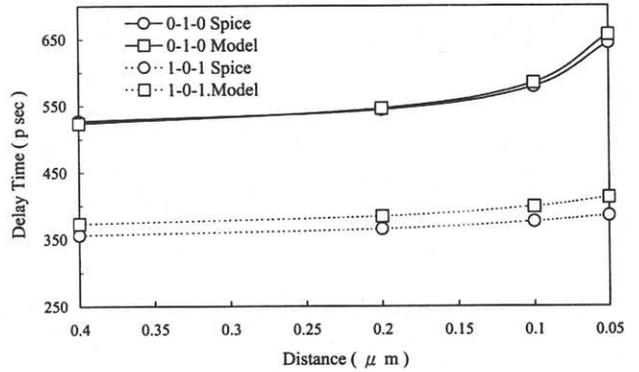


Fig. 3(b) Delay time using the 5-line model agrees with Spice for different distances between the bit lines.

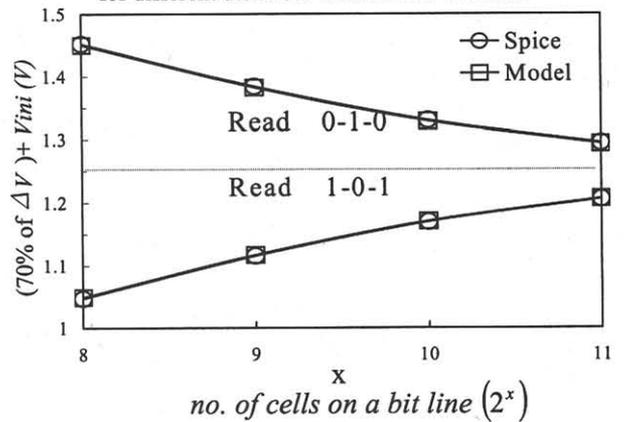


Fig. 4(a) V_0 reaching “(70% of ΔV) + V_{ini} ” using the 5-line model agrees with Spice for different no. of cells on a bit line.

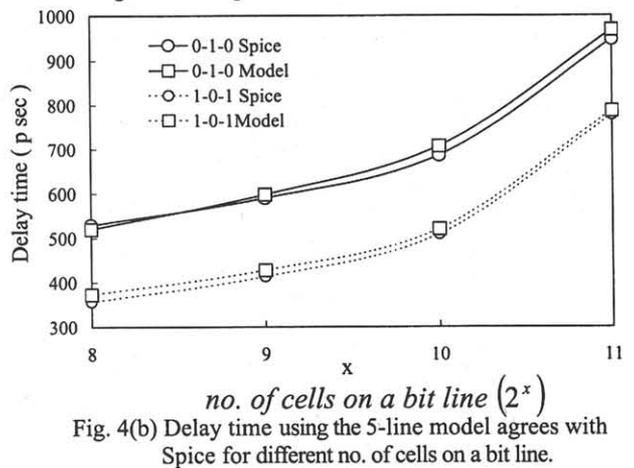


Fig. 4(b) Delay time using the 5-line model agrees with Spice for different no. of cells on a bit line.