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# The Vertical Replacement-Gate (VRG) MOSFET: A High-Performance Vertical MOSFET with Lithography-Independent Critical Dimensions

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## 1. Introduction

We have demonstrated a new device called the Vertical Replacement-Gate (VRG) MOSFET. This is the first MOSFET ever built in which 1) all critical transistor dimensions are controlled precisely without lithography, 2) the gate length is defined by a deposited film thickness, independently of lithography and etch, and 3) a high-quality gate oxide is grown on a single-crystal Si channel. In addition to this unique combination, the VRG-MOSFET includes self-aligned S/D extensions formed by solid source diffusion (SSD) and small parasitic overlap, junction, and S/D capacitances. The drive current per µm of coded width is larger than that of advanced planar MOSFETs because each device pillar (with a thickness of minimum lithographic dimension) contains two MOSFETs driving in parallel. All of this is achieved using current manufacturing methods, materials, and tools, and devices with 50-nm gate lengths  $(L_G)$  have been demonstrated without advanced lithography.

#### 2. Device Fabrication

The VRG process is different than all previous flows used to build vertical MOSFETs [1-4]. This process is outlined in Fig. 1 and is shown in more detail in Ref. [5]. Arsenic was implanted into an epi Si wafer to form the device drain and a thin oxide diffusion barrier was deposited. A PSG/nitride/undoped oxide/nitride/PSG/nitride stack was deposited and a trench (or window) with nearly vertical sidewalls was etched through the entire stack. The borondoped epitaxial Si device channel was grown selectively in this trench and the channel was planarized to the top nitride layer by CMP (Fig. 2). The undoped oxide film in the stack was a sacrificial layer whose thickness defined  $L_G$ , the two phosphosilicate glass (PSG) layers were dopant sources used to form low-resistance, shallow, self-aligned S/D extensions by SSD of phosphorus [6], and the thin nitride layers between the undoped oxide and the dopant sources functioned as etch stops and as precision offset spacers. A polysilicon source landing pad was deposited, implanted with arsenic, and patterned. After this landing pad and the top PSG dopant source had been encased in nitride, the sacrificial oxide layer was removed selectively to expose the vertical Si channel. A thin gate oxide was grown on the channel, and a phosphorous-doped, highly conformal a-Si gate was deposited and recrystallized. The TEM images of Fig. 3 show that the nearly perfect conformality of the a-Si deposition allowed it to fill the space underneath the top of the device without forming voids in the gate. The gate was patterned and backend processing was carried out.

The VRG-nMOSFET doping geometry was measured by scanning capacitance microscopy (Fig. 4). In the VRG process, the S/D extension lengths and gate overlaps are controlled by film thicknesses. The key enabling element of the VRG process is its replacement-gate approach - this allows for the fabrication of high-quality gate oxides on a

vertical {100} Si surface whose length is defined by a film thickness. This flow should be mechanically scalable to sub-30 nm gate lengths with excellent control. In Ref. [7], we describe an exemplary process for integrating n- and p-type VRG-MOSFETs to form side-by-side CMOS, which is comparable in density, parasitic capacitances, and process complexity to planar CMOS, while providing precise gate length control without lithography and up to twice the effective width for each transistor.

#### **3. Electrical Performance**

In addition to providing precise gate length control and new device design opportunities, the VRG process improves upon the performance of advanced planar MOSFETs. Figure 5 shows the subthreshold and  $I_D - V_{DS}$  characteristics of a 200-nm VRG-nMOSFET with  $t_{OX} = 28$  Å (physical). For  $V_{DD} = 2.5$  V, the drive current of this device normalized by its coded width  $W_C$  is 1.1 mA/µm - about 20% higher than that obtained for a planar MOSFET with the same  $L_{CH}$ ,  $t_{OX}$ , and  $I_{OFF} = 11$  pA/µm. The subthreshold swing s is 76 mV/decade. Straightforward improvements in series resistance and oxide processing should allow us to approach the ideal two-fold drive enhancement expected from having a MOSFET on either side of the Si pillar. The 50-nm device of Fig. 6 exhibits respectable short-channel performance at 1.5 V with DIBL = 90 mV, s = 105 mV/decade, and  $I_{OFF} = 13$ nA/µm at  $V_{GS} = V_T - 0.4$  V. Figure 7 illustrates that the gate leakage current density for an extremely wide VRG-MOSFET yield tester ( $W_c = 9060 \ \mu m$ ) is comparable to that of a planar MOSFET with the same  $t_{OX}$ . This suggests that in terms of the gate leakage current, VRG-MOSFET gate oxides can be shrunk well below 28 Å, and should be as scalable as those of planar MOSFETs.

## 4. Conclusions

We have demonstrated a unique vertical MOSFET aimed at high-performance logic and memory applications in which all critical transistor dimensions are controlled precisely without lithography. The VRG-MOSFET outperforms planar MOSFETs and creates new opportunities for continued scaling. Using production tools and without advanced lithography, we have fabricated 50-nm devices which have excellent DC characteristics, small parasitic capacitances, and low-leakage gate oxides.

#### References

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**Fig. 2.** TEM image of a 100-nm VRG-MOSFET after channel CMP.



**Fig. 4.** Scanning capacitance images of a 200-nm and a 50-nm VRGnMOSFET showing the self-aligned source/drain extensions formed by SSD and the two sides of the silicon pillar that drive in parallel.



**Fig. 6.** Subthreshold and  $I_D - V_{DS}$  characteristics of a 50-nm VRG-nMOSFET with  $t_{OX} = 28$  Å. This device was fabricated without advanced lithography using production tools and techniques.

Fig. 3. TEM image of a 100-nm VRG-MOSFET before gate etch and a blow-up of the active region showing the gate, the two nitride offset spacers, and a conservative 60 Å gate oxide.



**Fig. 5.** Subthreshold and  $I_D - V_{DS}$  characteristics of a 200-nm VRGnMOSFET with  $t_{OX} = 28$  Å.  $I_{ON} = 1.1$  mA/µm,  $\approx 20\%$  higher than that of a planar MOSFET with the same  $L_{CH}$ ,  $t_{OX}$ , and  $I_{OFF} = 11$  pA/µm.



Fig. 7. Comparison of VRG and planar MOSFET gate leakage. In terms of gate leakage, VRG-MOSFET gate oxides can be scaled well below 28 Å.