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# Study on Zr-Silicate Interfacial Layer of $ZrO_2$-MIS Structure Fabricated by Pulsed Laser Ablation Deposition Method

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## 1. Introduction

The $ZrO_2$ high-k dielectric has been investigated as a view to its application as a replacement for $SiO_2$ in sub-100 nm CMOS technology; however the unavoidable appearance of the interfacial layers between the high-k gate dielectrics and Si substrate have been reported [1]. Though the dielectric properties of interfacial layer are important for the sub-2 nm equivalent oxide thickness (Teq), required for the advanced CMOS technology, these properties have not been clarified yet.

In this study, the properties of the interfacial layer of $ZrO_2$-MIS structures fabricated by the Pulsed Laser ablation Deposition (PLD) method [2], which is a method controllable independently of deposition parameters, i.e., substrate temperature and gas pressure, were investigated. For the first time, we successfully evaluated the dielectric properties of the interfacial layers directly, which were confirmed to be Zr-silicate structures by physical analysis.

## 2. Experimental

The $ZrO_2$ films were deposited on the Si substrates with diluted HF treatments by the PLD method at various substrate temperatures between 200 ℃ and 800 ℃. $O_2$ gas pressure was 0.2 Torr. $ZrO_2$-MIS structures with the various $ZrO_2$ thicknesses with the same thermal budgets are also fabricated, in order to evaluate the dielectric properties of interfacial layers and $ZrO_2$ layers separately.

## 3. Results and discussion

A cross-sectional TEM image of the interface of $ZrO_2$-MIS capacitor is shown in Fig.1. This image clearly shows the formation between $ZrO_2$ and Si substrate of the amorphous interfacial layer having a thinness of as little as 1nm. The C-V and J-V characteristics of this capacitor are shown in Fig. 2. Teq is about 1.3 nm estimated from the accumulation capacitance measured by the two-frequency C-V method [3]. This $ZrO_2$ MIS exhibits the negligible frequency dispersion between 50 kHz and 600 kHz and negligible hysteresis (Fig. 3). The leakage current density is about $10^{-2}$ A/cm$^2$ at the gate voltage of -2V, which is much smaller than that of $SiO_2$ film of the same Teq ($J_{SiO2} \sim 10^2$A/cm$^2$). However, since the physical thickness of the interfacial layer occupies more than half of the equivalent thickness, it is unquestionable that dielectric properties of these interfacial layers are so critical for the realization of the thinner dielectrics.

Firstly we investigated the structural properties of interfacial layer by using the EDX and XPS analysis. Zr atoms were detected in the region close to the Si surface (Fig. 3). The average composition of Zr in the interfacial layer of 4~5 at% was obtained from both of the EDX and XPS analysis. Figure 4 shows the binding energy profiles of the interfacial layer that was remained by the etching of $ZrO_2$ layer. For the comparison, the results of $ZrO_2$ and $SiO_2$ are also shown. Whereas the Zr-Si bonds were not detected, Zr-O and Si-O bonds of the interfacial layer were detected at the same binding energy with $ZrO_2$ and $SiO_2$, respectively. Thus, we concluded that the interfacial layer of $ZrO_2$-MIS capacitor is Zr-silicate layer.

Next, we evaluated the dielectric constants (ε) of the silicate layer and $ZrO_2$ layer separately, by using the MIS capacitors with various $ZrO_2$ thicknesses, for a given silicate thickness that were confirmed by TEM observations. The schematic image of this evaluation method is shown in Fig. 5. The slope shows the $1/\varepsilon_{ZrO2}$, and $\varepsilon_{Silicate}$ is evaluated from the intercept value of $1/C$. Then, using these methods, the effects of deposition temperatures on each dielectric constant have been investigated. Figure 6 shows the dielectric constants of the MIS capacitors fabricated at the different deposition temperature and with the equal thermal budgets. The $\varepsilon_{ZrO2}$ are almost the same, however, $\varepsilon_{silicate}$ of MIS capacitor fabricated at 200 ℃ (~5) is much lower than that of MIS capacitor fabricated at 600 ℃ (~9), even if the thermal budget is identical. This fact means that the dielectric constant of the silicate layer of MIS capacitor is sensitive to the $ZrO_2$ deposition temperature.

Finally, we report the direct evaluation of the dielectric properties of the interfacial silicate layer of MIS capacitor. The $ZrO_2$ layer of MIS capacitor was removed by the HF etching after the fabrication of $ZrO_2$-MIS capacitor at 500 ℃. Due to the difference in etching rate between $ZrO_2$ and the silicate layer (Fig. 7), only the silicate layer remained. In order to recover the etching damage, the remained silicate layer was annealed at 600 ℃ for 5 min. in dry $O_2$ atmosphere. Figure 8 shows that the remained silicate film of as thin as 1.9nm after annealing. The C-V characteristic of the Zr-silicate MIS capacitor is shown in Fig. 9. This silicate MIS capacitor also exhibits the negligible frequency dispersion and hysteresis. Teq is 0.9 nm obtained from the accumulation capacitance of the two-frequency C-V method. The value of $\varepsilon_{Silicate}$ is estimated to be 8 that is slightly smaller than the $\varepsilon_{Silicate}$ evaluated from the above method (Fig. 6), which may be due to the recovering annealing. Thus, we could evaluate only the ultra-thin interfacial silicate layer of $ZrO_2$-MIS capacitor directly.

## 4. Conclusion

. We successfully investigated both the physical and the dielectric properties of only the interfacial Zr-silicate layer of $ZrO_2$-MIS capacitor. The ultra-thin interfacial Zr-silicate MIS capacitor with Teq of 0.9 nm and ε of 8 was successfully evaluated. It was also clarified that the dielectric constant of the interfacial silicate layer of $ZrO_2$-MIS capacitor depends on the deposition temperature even with keeping the thermal budgets to be equal.

## Acknowledgment

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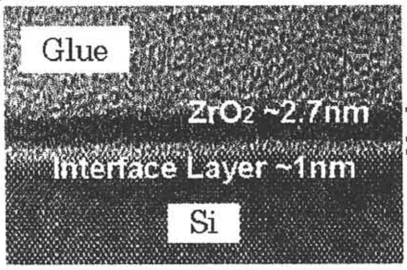


Fig.1 Cross-sectional TEM image of $ZrO_2$-MIS capacitor fabricated at 500 ℃, 5 min. , in $O_2$.

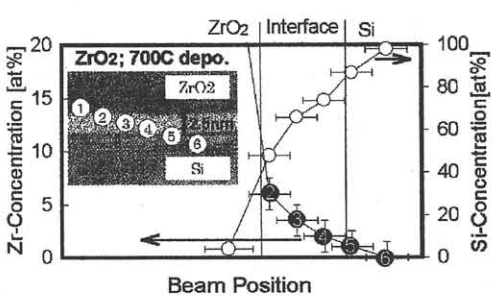


Fig. 3 Composition profiles in the interfacial layer of $ZrO_2$-MIS capacitor fabricated at 700℃ detected by EDX. Inset numbers correspond to the scanning beam position of EDX.

## Reference

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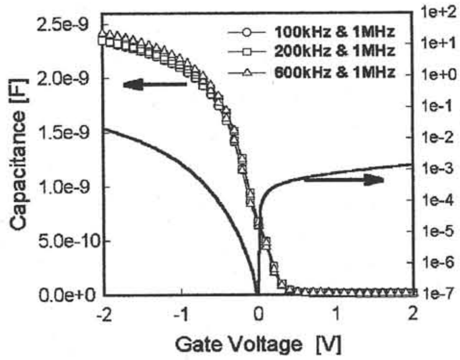


Fig. 2 C-V characteristics of $ZrO_2$-MIS capacitor by using the two-frequency method, indicating the negligible frequency dispersion and hysteresis. J-V characteristics is also shown.

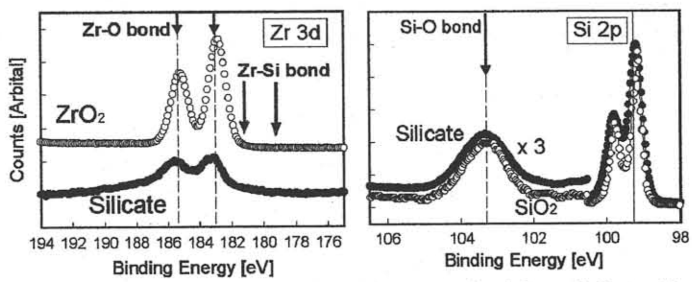


Fig. 4 XPS spectra of the interfacial layer remained through the etching of $ZrO_2$ layer, indicating the suitable bonding structures to the silicate structures.

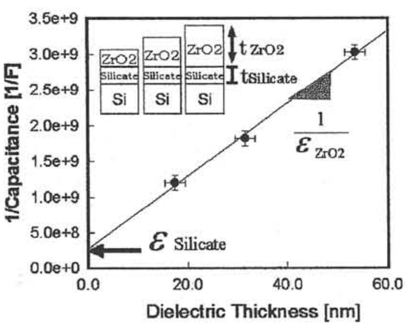


Fig. 5 Schematic image of the method of evaluating $\varepsilon_{ZrO2}$ and $\varepsilon_{Silicate}$, separately.

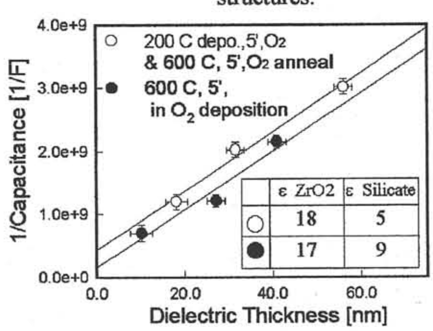


Fig. 6 The dependence of deposition temperature on $\varepsilon_{ZrO2}$ and $\varepsilon_{Silicate}$ of the MIS capacitors with equal thermal budgets.

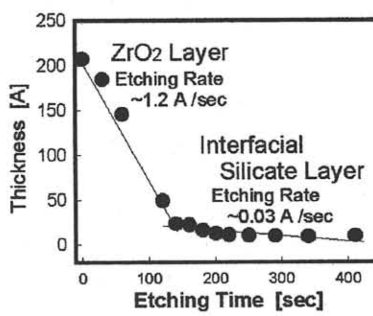


Fig. 7 Different etching rate of $ZrO_2$ layer and the silicate layer to enable only the interfacial silicate layer to be remained.

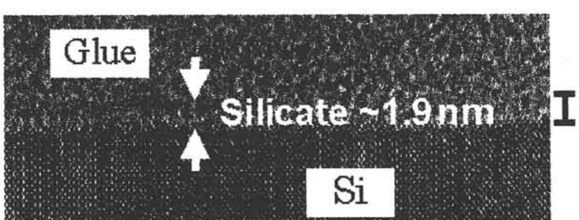


Fig. 8 Cross-sectional TEM image of the remained interfacial silicate after etching of $ZrO_2$ layer that was deposited at 500 ℃, which are annealed at 600 ℃, 5 min., in $O_2$.

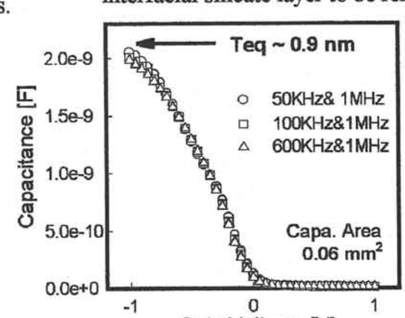


Fig. 9 HF C-V characteristics of the silicate-MIS capacitor with Teq of 0.9 nm and $\varepsilon_{Silicate}$ of 8, indicating the negligible frequency dispersion and hysteresis.