Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 230-231

B-5-3

Charge Trapping in SiO_x/ZrO_2 Gate Dielectric Stacks

M. Houssa[(1,2)], M. Naili[(2)], M.M. Heyns[(2)], and A. Stesmans[(1)]

[(1)]Department of Physics, Katholieke Universiteit Leuven, Celestijnenlaan 200 D, B-3001 Leuven, Belgium.
[(2)]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium.
Phone: +32 16 32 72 26 Fax: +32 16 32 79 87 E-mail: michel.houssa@fys.kuleuven.ac.be

1. Introduction

The trapping of charge carriers in very thin SiO_x/ZrO_2 gate dielectric stacks is studied. The trap generation rate and the cross section of electron traps generated in these gate stacks are extracted from the analysis of the increase of the current density observed during constant voltage stress of MOS capacitors. All the results can be consistently explained by a model based on a two stage degradation process, i.e. 1) H^+ release in ZrO_2 by the injected electrons and 2) transport of H^+ in the ZrO_2 layer, resulting in bond breaking and generation of ZrOH neutral trapping centers.

2. Experimental

ZrO_2 layers were deposited by ALCVD at 300 °C using $ZrCl_4$ and H_2O as sources [1] on n-type (100) Si wafers. The wafers had an ultra-thin chemical SiO_x layer of the order of 1 nm on top of the Si substrate prior to the deposition of the high permittivity dielectric layers. MOS capacitors were defined on the gate dielectric stacks by evaporating gold dots ($5x10^{-3}$ cm^2) through a shadow mask.

3. Results and discussion

The J-V characteristics of a 1.1nm SiO_x/7.4 nm ZrO_2 stack recorded after different time during constant gate voltage stress (substrate injection) are shown in Fig.1. One observes that J_G increases with increasing stress time at low voltage. This contribution is the stress-induced leakage current (SILC) and is due to trap-assisted tunneling through neutral electron traps generated in the gate dielectric during the stress [2]. The increase of the current density $\Delta J(t)=J(t)-J(0)$ during constant voltage stress is shown in Fig.2 for different values of V_G. One observes that the current increases with time, and that this relative increase is more important as V_G is increased. The time-dependent gate current density can be modelled by the expression [3]

$$\Delta J(t,V_G)=A(1-Exp[-(t\,\sigma J_{inj})/q])+\beta(V_G)\,t^{\delta} \qquad (1).$$

The first term of Eq.(1) accounts for the build-up of charges in the gate dielectric, where σ is the trap cross section and J_{inj} the current density injected into the gate dielectric during the stress and the second term takes into account the SILC contribution to the gate current which increases with time according to a power law [4] with $\beta(V_G)$ the trap generation rate. Solid lines in Fig.2 are fits to the data using Eq.(1); σ and β can be extracted from these fits.

The normalized trap generation rate $\alpha=(\beta\, t^{\delta}_{stress})/Q_{inj}$ is shown in Fig.3 as a function of V_G for a 1.1 nmSiO_x/7.4 nm ZrO_2 gate stack as well as for a reference thermal (2.7 nm) SiO_2 layer. One observes that α varies exponentially with V_G and that the relative increase in α is reduced in the SiO_x/ZrO_2 stack as compared to the SiO_2 layer. These results can be explained by the following two step degradation model [5-7]: electrons tunneling through the gate stack and arriving at the anode with an energy qV_G (ballistic regime) may release H^+, provided that qV_G is larger than the threshold energy E_{th} for H^+ generation in the gate dielectric. The protons are next accelerated toward the cathode by the electric field E in the gate dielectric, leading to the breaking of bridging O bonds and the trapping of H^+ at the resulting ZrO or SiO sites. This model leads to the following epression for α

$$\alpha=\alpha_o Exp[(qV_G-E_{th})/E_{th}]Exp[(ql_{hop}E-E_a)/k_BT] \quad (2)$$

where l_{hop} is the hopping distance for H^+ transport in the gate dielectric [5] (see Table I) and E_a is the activation energy for H^+ transport and bond breaking. The solid lines in Fig. 3 are fits to the data using Eq.(2) with E_{th} as a free parameter (see Table I). The agreement between the data and the model is excellent. The smaller relative increase of α in SiO_x/ZrO_2 can be explained by the fact that the electric field E in the high permittivity dielectric is much smaller than in the thermal SiO_2 layer, leading to the reduction of H^+ diffusion and bond breaking in the high permittivity gate stack.

The temperature dependence of $\Delta J(t)$ in the ZrO_2 gate stack is illustrated in Fig.4. From these data, the temperature dependence of α can be extracted using Eq.(1); α is presented in Fig. 5 as a function of 1/T. Solid lines are fits to the data using Eq.(2) with E_a as a fitting parameter (Table I). One can see that the temperature dependence of α is also consistent with the degradation model discussed above.

The trap cross sections σ extracted from Fig. 2 are given in Table I for SiO_x/ZrO_2 and SiO_2. The quite small value of σ in the high permittivity gate stack suggests that traps are most probably generated in the ZrO_2 layer. As a matter of fact, the cross section of a neutral center with polarizability α_D in a medium of dielectric constant ε varies like $\sigma\sim(\alpha_D/\varepsilon^2)^2$ [8]. The trap cross section σ is presented in Fig. 6 as a function of the ratio α_D/ε^2 on a log-log scale (data obtained on a TiO_2 gate stack are also shown). Consistently with the model discussed above, we assumed that the neutral traps generated in the gate delectric are respectively SiOH, ZrOH and TiOH centers (the values of α_D and ε are given in Table I). From Fig. 6, one can see that σ behaves like a power law with (α_D/ε^2), with an exponent equal to 2.06±0.01. The agreement between the experimental results and theory is very good and suggests that traps generated during the stress of the high permittivity gate stacks are ZrOH or TiOH neutral centers.

4. Conclusions

The trapping of charge carriers during constant voltage stress of SiO_x/ZrO_2 gate dielectric stacks has been investigated. We have shown that the trap generation rate in these gate stacks can be explained by a degradation model which takes into account the release of H^+ protons close to the anode by the injected electrons and the subsequent transport of H^+ in the high permittivity dielectric, resulting in bond breaking and trap generation. The cross section σ of these trapping centers has been estimated to be about $2x10^{-18}$ cm^2. From the analysis of σ, we have shown that these neutral traps are probably ZrOH centers generated during the transport of H^+ in the ZrO_2 layer.

References

[1] M. Copel, M. Gribelyuk, and E. Gusev, Appl. Phys. Lett. **76**, 436 (2000).

[2] J. De Blauwe, J. Van Houdt, D. Wellekens, G. Groeseneken, and H. Maes, IEEE Trans. Electron Devices **45**, 1745 (1998).

[3] T. Nigam, R. Degraeve, G. Groeseneken, M.M. Heyns, and H. Maes, *Proc. 37th Intern. Reliab. Phys. Symp.* (IEEE, Piscataway, 1999), p.381.

[4] K. Okada, H. Kubo, A. Ishinaga, and K. Yoneda, *Techn. Digest of VLSI Symp,* (IEEE, Piscataway, 1998), p. 158.

[5] F.B. McLean, IEEE Trans. Nucl. Sci. **37**, 1624 (1990).

[6] D. Arnold, E. Cartier, and D.J. DiMaria, Phys. Rev. B **49**, 10278 (1994).

[7] V. Afanas'ev and A. Stesmans, J. Electr. Soc. **146**, 3409 (1999).

[8] K.C. Kao and W. Hwang, *Electrical Transport in Solids* (Pergamon Press, London, 1981).

Table I. Hopping distance for H^+ transport (l_{hop}), electron threshold energy for H^+ release (E_{th}), activation energy for H^+ transport (E_a), trap cross section (σ), polarizability of OH related centers (α_D) and dielectric constant (ε) of SiO_2 and SiO_x/ZrO_2 gate dielectric layers.

Sample	l_{hop} (Å)	E_{th} (eV)	E_a (eV)	σ (cm^2)	α_D ($Å^3$)	ε
SiO_2	2.5	1.4	0.6	$1.5x10^{-16}$	3.13	3.9
SiO_x/ZrO_2	2.8	1.1	0.5	$2.0x10^{-18}$	5.51	15.3

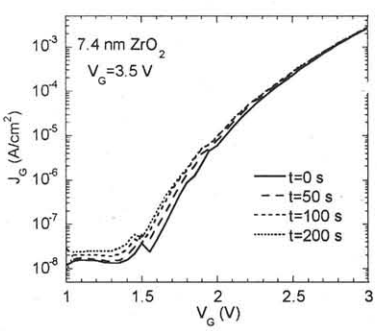

Fig. 1. Current-voltage characteristics of a 7.4 nm ZrO_2 layer recorded after different time during constant gate voltage stress at 3.5 V.

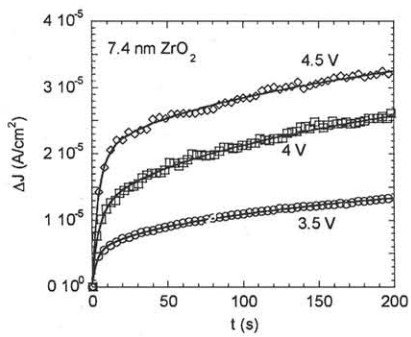

Fig. 2. Time-dependence of the current density increase ΔJ of a 7.4 nm ZrO_2 layer. Solid lines are fits to the data obtained by using Eq.(1).

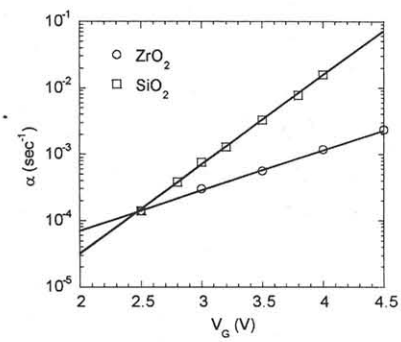

Fig. 3. Trap generation rate α vs gate voltage stress of a 7.4 nm ZrO_2 layer and a 2.7 nm SiO_2 layer. Solid lines are fits to the data using Eq.(2).

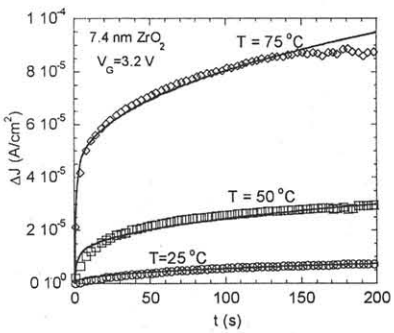

Fig. 4. Time dependence of the current density increase ΔJ of a 7.4 nm ZrO_2 layer from room temperature up to 75 °C. Solid lines are fits to the data using Eq.(1).

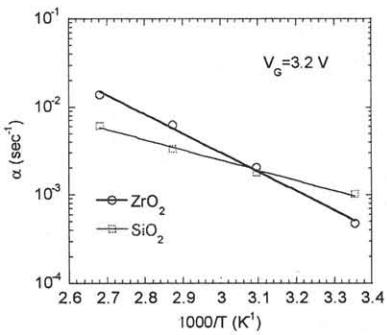

Fig. 5. Trap generation rate α as a function of the inverse of temperature of a 7.4 nm ZrO_2 layer and a 2.7 nm SiO_2 layer. Solid lines are fits to the data using Eq.(2).

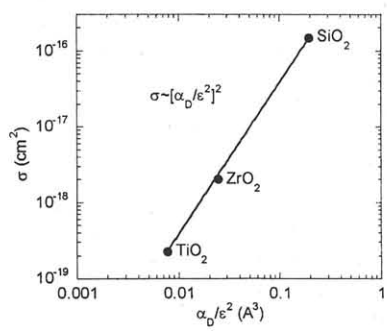

Fig. 6. Trap cross section σ as a function of the ratio (α_D/ε^2) on a log-log scale for SiO_2, ZrO_2 and TiO_2 gate layers. The solid line is a power law fit.