# B-5-4

# Chemical Bonding at Interfaces between Si (100) and High-K Dielectrics: Competing Effects of i) Process Gas-Substrate and ii) Film Deposition Reactions

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# 1. Introduction

The substitution of alternative gate dielectrics for SiO<sub>2</sub> necessitates a fundamental change in processing from thermally-grown dielectrics with interface formation occurring during growth, to deposited dielectrics with interfaces either being formed during film deposition, or during a separate and independent processing step. Experience to date with deposited SiO<sub>2</sub> has indicated the necessity of a separate interface formation step to suppress subcutaneous oxidation of the Si substrate which can occur during film deposition [1]. We have previous demonstrated that stacked gate dielectrics comprised of plasma processed nitrided Si-SiO<sub>2</sub> interfaces, and Si nitride and oxynitride alloys prepared by remote plasma-enhanced chemical vapor deposition, RPECVD, could be used to reduce direct tunneling by up to three orders of magnitude with respect to devices with SiO<sub>2</sub> dielectrics, and thereby extend the equivalent oxide thickness, EOT, from ~1.6 nm to ~ 1.1 nm [1]. This paper extends these studies to alternative gate dielectrics that have been proposed high-k replacements for SiO2. Interfacial reactions that either form metal-silicide bonds, e.g., Si-Ta, Si-Zr, etc., or metal silicate alloys, e.g.,  $Zr_xSi_{1-x}O_4$ , etc., can occur during deposition. We have studied three different high-k dielectrics in which there are fundamental differences between silicate alloys along the pseudo-binary joins between SiO<sub>2</sub> and the respective metal oxides, Ta<sub>2</sub>O<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>. Specifically: i) there is no stoichiometric compound silicate the SiO<sub>2</sub>-Ta<sub>2</sub>O<sub>5</sub> system, so that alloys along this join are solid solutions with random oxide bonding; ii) there are two stoichiometric silicates in the  $SiO_2$ -Al<sub>2</sub>O<sub>3</sub> system in which AlO<sub>4/2</sub> and SiO<sub>4/2</sub> groups form a random network in which negative charge on the Al-groups is compensated by Al<sup>3+</sup> ions: and finally, iii) there is a stoichiometric silicate,  $ZrSiO_4$ , in the  $SiO_2$ - $ZrO_2$  system in which there are  $Zr^{4+}$  ions and  $SiO_4$  silicate ions.

## 2. Experimental Procedures

Interfaces and films for these studies were prepared by remote plasma-processing techniques that have been discussed at length elsewhere, e.g., in Ref. 1. The studies relied on in-line Auger electron spectroscopy, AES, to identify the evolution of interface bonding arrangements. This technique is particularly well-suited for these studies because of the relative short escape depths of the Auger electrons associated with the different atomic species, e.g., from  $\sim 0.6$  nm for Si<sub>LVV</sub> features to about 1.0 nm for N<sub>KLL</sub> and O<sub>KLL</sub> features. Dielectrics were deposited onto Si(100)

surface from which sacrificial thermal oxides had been removed by etching in dilute HF. Figure 1 indicates AES spectra for initial stages of  $Ta_2O_5$  and  $SiO_2$ - $Ta_2O_5$  alloy deposition. There is no evidence for formation of  $SiO_2$ - $Ta_2O_5$  alloys during the  $Ta_2O_5$  deposition.



Fig. 1. AES spectra for Si-Ta<sub>2</sub>O<sub>5</sub> and Si-(SiO<sub>2</sub>-Ta<sub>2</sub>O<sub>5</sub> alloy) interfaces.

Figure 2 present similar AES for the formation of Si(100)-Al<sub>2</sub>O<sub>3</sub> interfaces. There is no evidence for Si-O bonds except at the initiation of the plasma deposition process in which the film thickness, estimated from the AES features, is < 0.8 nm.



Figure 3 present TEM micrographs for the deposition of  $SiO_2$ -rich alloys in the  $SiO_2$ -ZrO<sub>2</sub> system. There is no discernable difference between the two micrographs: i) for

deposition directly onto HF-last Si(100), and ii) for deposition on an  $\sim 0.6$  nm SiO<sub>2</sub> interfacial layer formed by remote plasma-assisted oxidation of the Si substrate [1].



Fig. 3. TEM micrographs for SiO<sub>2</sub>-ZrO<sub>2</sub> deposition: (a) onto HF-last Si, and (b) onto SiO<sub>2</sub>.

#### 3. Discussion

The results in Figs 1 and 2 indicate no significant silicate formation during the deposition of either i)  $Ta_2O_5$  or ii)  $Al_2O_3$  onto Si(100) by remote plasma deposition. For each of these depositions, an  $O_2$ /He mixture was plasma-excited and active species were delivered to the substrate from a remote plasma-activation tube (see Ref. 1). The process gases, Ta-ethoxide, and Al-TEDA-TSB [2], were injected downstream from the plasma and were note directly excited. The substrate temperature was 300C for each of the depositions and the process pressure was 300 mTorr, which is sufficient to contain the plasma in the excitation tube.

The TEMs of Fig. 3 are consistent with substrate reactions in which  $SiO_2$ -Zr $O_2$  alloys are formed at both Si and  $SiO_2$  substrates during film deposition. The bi-layer character of the TEM images is consistent with these interface layers have a composition different than that of the deposited Zr-silicate alloy film.

The combined results in Figs. 1-3 indicate that interfacial silicate formation during the strongly oxidizing conditions of RPECVD deposition is qualitative different for i) Ta<sub>2</sub>O<sub>5</sub>, SiO<sub>2</sub>-Ta<sub>2</sub>O<sub>5</sub> alloys and Al<sub>2</sub>O<sub>3</sub> and ii) SiO<sub>2</sub>-ZrO<sub>2</sub> alloys. In direct contrast, interfacial Al<sub>2</sub>O<sub>3</sub>-SiO<sub>2</sub> alloy layers were formed by the CVD deposition of Al<sub>2</sub>O<sub>3</sub> onto HF-last silicon using the same Al-precursor of this study [2]. SiO<sub>2</sub> and/or SiO<sub>2</sub>-ZrO<sub>2</sub> alloy layers are formed on Si(100) during the CVD deposition of ZrO<sub>2</sub> onto HF-last silicon as well [3].

Electrical measurements on nMOS and pMOS capacitors (MOSCAPs) have provided some additional information relative to the quality of interfacial layers that are formed at the initial stages of film deposition. For n- and p-MOSCAPs with Ta<sub>2</sub>O<sub>5</sub> dielectrics in an EOT range from 1 to 1.3 nm, C-V and I-V measurements indicate negative shifts flat band voltage shifts of  $\sim 0.1$  eV for direct deposition of Ta<sub>2</sub>O<sub>5</sub> onto HF-last Si, as compared to devices with 0.6 nm plasma-oxides. All devices were annealed at 800C prior to deposition of gate electrodes. In addition, devices with monolayer nitrided SiO<sub>2</sub> interface layers showed 10-fold reductions in tunneling current, paralleling

results for deposition of SiO<sub>2</sub> and Si-nitride and oxynitride onto the same interface layers [1]. Finally, the flat band voltages of devices with nitrided and non-nitrided SiO<sub>2</sub> interface layers were the same to less than 0.005 V as those in devices fabricated on the same Si substrates with SiO<sub>2</sub> deposited dielectrics [1]. The poorer performance for devices formed by direct deposition onto HF-last Si is consistent with XPS studies that have demonstrated that metallic Ta-Si bonds form during 800C anneals due to an inherent interface chemical instability [4]. The oxides and silicates of Al and Zr are stable on Si, so that similar reactions are neither anticipated nor observed [5].



Fig 4. C-V traces of n- and p-MOSCAPs

Finally, devices fabricated on HF-last and plasmaoxidized substrates with  $SiO_2$ -ZrO<sub>2</sub> showed relatively small differences in flat band voltage and hysterisis.

Combining i) in situ and ex-situ characterizations of Sihigh-k dielectric interfaces and ii) electrical measurements has highlighted important issues for the utilization of high-k dielectrics in aggressively-scaled devices. First, there are significant differences between interface reactions that can be correlated with the existence of, and bonding in compound silicate phases. Second, interface reactions are generally deposition process dependent. Finally, in many instances, it will necessary to use thin interfacial nitrided SiO<sub>2</sub> interface layers to reduce interfacial defects. These will have a significant effect on the attainable EOTs values due their effect on the physical thickness of the high-k dielectric.

## Acknowledgments

Sponsored by the ONR, SRC and the SEMATECH/SRC FEP center. We acknowledge support from Motorola Corp. in the providing the TEM images.

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