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TaO_xN_y Gate Dielectric with Improved Thermal Stability

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ABSTRACT

We report characteristics of TaO_xN_y gate dielectric with improved thermal stability and favorable flat band shift over Ta_2O_5 for giga scale memory devices. Compared with Ta_2O_5, $W/WN/TaO_xN_y/SiO_2/Si$ *n*MOS capacitors demonstrated negative V_{fb} shift (-0.17 V) and robust reliability against selective oxidation at 950℃. Interface state density (D_{it}) as low as 8.5～15 x 10^{10} $eV^{-1}cm^{-2}$ near the midgap and excellent reliability characteristics with low gate leakage current are encouraging for future memory devices.

INTRODUCTION

Ta_2O_5 has attracted lots of attention for MOS device applications such as storage capacitors[1] and gate dielectrics[2-5] because of high dielectric constant (k～25) and good leakage current. There are some problems, however, such as chemical reaction between Ta_2O_5 and poly-Si, which led to the employment of stable electrodes such as refractory metal or metal nitrides [1-4]. Owing to the high work function of metal nitrides, it is difficult to obtain low threshold voltage in MOSFET device [4,5]. In addition, the fragility of metal/Ta_2O_5 structure against post thermal budget in oxidation ambient becomes a serious issue for device reliability and requires new fabrication scheme. In the present work, we implemented a novel process to overcome the problems associated with threshold voltage and thermal stability using TaO_xN_y gate dielectric.

EXPERIMENTAL

*n*MOS capacitors and transistors having W/barrier metal/Ta_2O_5/SiO_2/p-Si structure were fabricated. Ta_2O_5 was deposited on the ultrathin (~5-10 Å) SiO_2 using $Ta(OC_2H_5)_5$ and O_2 at 400℃, whereas TaO_xN_y was prepared using $Ta(OC_2H_5)_5$ and NH_3[6]. Gate dielectric improvement anneals were carried out in ultraviolet-ozone at 350℃ and in O_2 at 800℃. Then, W/barrier metal (TiN or WN) electrodes were sputter-deposited on gate dielectric and annealed in N_2 at 700-800℃ for 30 minute. In order to investigate the effect of selective oxidation (SO) on gate dielectric, samples were oxidized in H_2-rich oxidant ambient at 950℃ for 2 minute. Fundamental film properties were probed by X-ray photoelectron spectroscopy (XPS) and auger electron spectroscopy (AES). Interfacial and electrical properties of W/barrier/TaO_xN_y/SiO_2/Si MOS capacitors were measured using C-V, conductance, I-V, breakdown voltage (BV), and time dependent dielectric breakdown (TDDB) methods.

RESULTS AND DISCUSSIONS

A. W/Metal barrier/Ta_2O_5/SiO_2/Si nMOS System

Shown in Fig. 1 is leakage current density of Ta_2O_5 film with different metal gate electrode, where WN exhibited lower gate leakage than TiN near 2-3 V range after anneal at 700℃～800℃. Fig. 2 shows sharp WN/Ta_2O_5 interface as detected by XPS core level spectra, confirming stable WN with Ta_2O_5 at elevated temperature. We observed interfacial reaction at TiN/Ta_2O_5 interface, however, due to the solubility of Ta in TiN [1]. A projected 10-year lifetime of WN/Ta_2O_5 (Fig.3) as determined by TDDB under the constant stress reveals superior lifetime to the thermal oxide. An electric field of over ~10 MV/cm may be used at room temperature using WN/Ta_2O_5. Fig. 4 displays the threshold voltage (V_{th}) of metal gated Ta_2O_5/SiO_2/Si nMOSFET with high V_{th}(～1V), which is consistent with the earlier works [4,5].

B. W/WN/TaO_xN_y/SiO_2/Si nMOS System

In order to reduce V_{th} by controlling charges in gate dielectrics, we developed TaO_xN_y gate dielectric. Fig. 5 depicts high frequency C-V plots with TaO_xN_y, demonstrating negative shift (-0.17 V) in flat band condition with respect to Ta_2O_5 and small hysteresis (20 mV). The AES depth profiles of TaO_xN_y films in Fig. 6 indicate that nitrogen was diffused out or piled up at SiO_2/Si interface after improvement anneal. The negative flat band shift is attributed to the N induced positive charges, resulting in a favorable V_{th} for high performance nMOSFET. Figs. 7-8 are high-low C-V and G/ω -log ω plots of W/WN/TaO_xN_y/SiO_2/Si nMOS capacitors after anneal in forming gas. Excellent frequency dispersion between 1 MHz and 100Hz except the midgap region is observed. The D_{it} as determined by conductance loss (G/ω) near the midgap including small hump region is in the order of 8.5～15x10^{10} $eV^{-1}cm^{-2}$. Fig. 9 displays J-V characteristics of TaO_xN_y and Ta_2O_5 at the same T_{eff}~31 Å, where the gate leakage of TaO_xN_y is ~5 orders of magnitude lower than that of poly-gated SiO_2 at -2.5 V. The highlight of this work is improved thermal stability using TaO_xN_y even after SO at 950℃ (Figs.10-11). TaO_xN_y showed durable reliability characteristics over Ta_2O_5 in terms of less increase in T_{eff} (Fig.10) and higher BV pass rate on 64 million memory cell capacitors (Fig.11). Excellent BV distribution (11 MV/cm) of TaO_xN_y film even after selective oxidation indicates that TaO_xN_y film may allow us to keep up the standard CMOS fabrication process and technology.

CONCLUSIONS

WN gate electrode demonstrated stable interface with Ta_2O_5 at the elevated temperature over TiN. Compared with Ta_2O_5, TaO_xN_y gate dielectric exhibited good-natured negative V_{fb} shift and durability against high temperature selective oxidation. Characteristics such as low D_{it}, low gate leakage current, and excellent reliability are promising for future DRAM devices.

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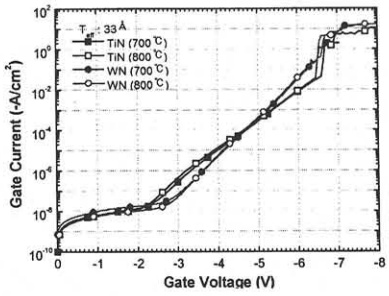

Fig. 1. J-V characteristics of Ta_2O_5 with TiN and WN barrier metal as a function of post thermal budget.

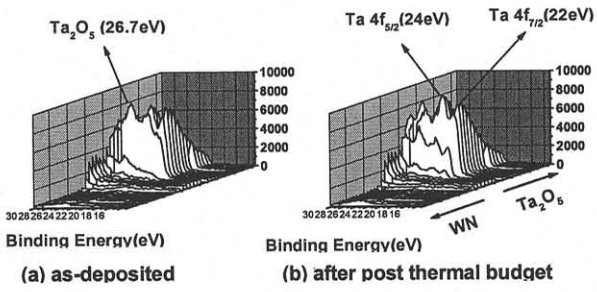

Fig. 2. XPS core level spectra near the WN/Ta_2O_5 interface with post thermal budget.

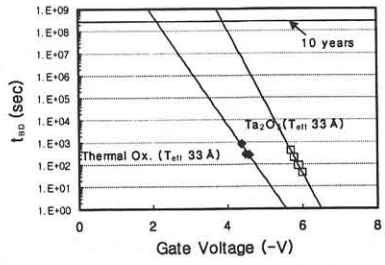

Fig. 3. Time to 50% cumulative failure of $W/WN/Ta_2O_5/SiO_2/Si$ nMOS capacitor.

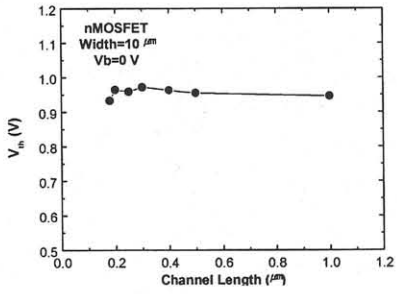

Fig. 4. V_{th} of metal gated $Ta_2O_5/SiO_2/Si$ nMOSFET as a function of channel length.

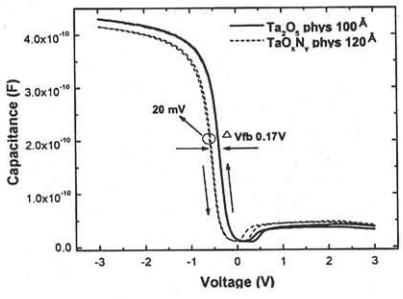

Fig. 5. Hysteresis curves of Ta_2O_5 and TaO_xN_y nMOS capacitors.

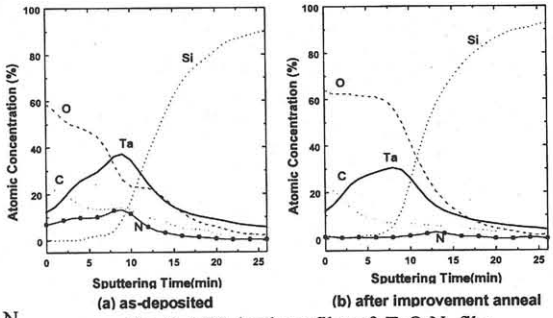

Fig. 6. AES depth profiles of TaO_xN_y film.

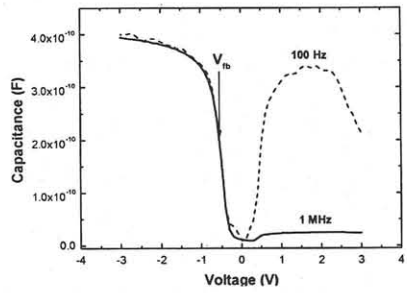

Fig. 7. High-low C-V characteristics of WN/W $TaO_xN_y/SiO_2/Si$ nMOS capacitor.

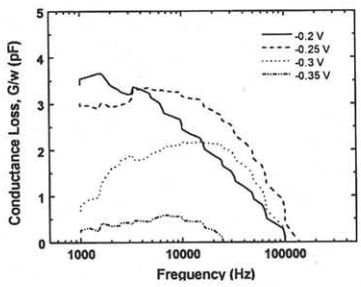

Fig. 8. Conuctance loss (G/ω) - log ω plot as a function of gate voltage near the midgap.

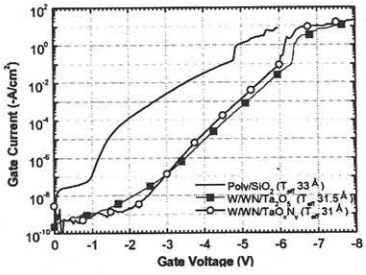

Fig. 9. J-V characteristics of Ta_2O_5 and TaO_xN_y films compared with controlled oxide.

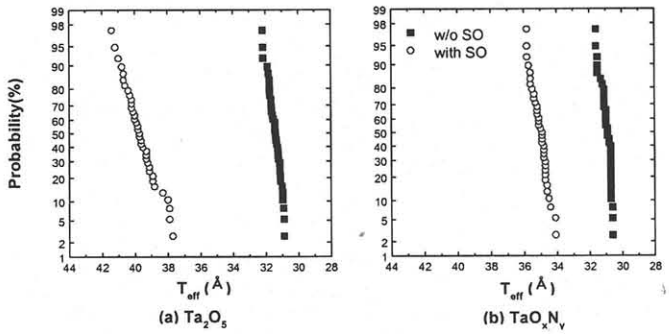

Fig. 10. T_{eff} change after selective oxidation.

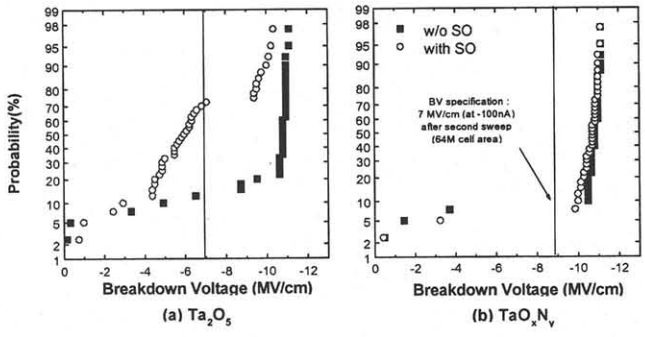

Fig. 11. Cumulative probability of breakdown field on 64 M cell area.