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Intrinsic Limitations on Ultimate Device Performance and Reliability from Transition Regions at i) Si-Dielectric Interfaces and ii) Internal Interfaces

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1. Introduction

This paper describes a newly identified interface bonding effect that places intrinsic limitations on the abruptness of semiconductor-dielectric and internal dielectric interfaces in semiconductor devices, thereby limiting the ultimate performance and reliability in advanced Si CMOS devices. As channel lengths in these devices are scaled to <100 nm, and the equivalent oxide thickness (EOT) of gate dielectrics is proportionally scaled down to <1.5 nm, process and stress-induced bonding defects in these transition regions pose a significant limitation on performance and reliability. This paper i) presents experimental evidence for mono-layer-scale transition regions at Si-SiO_2 interfaces [1-3]; ii) discusses device performance and reliability in PMOS and MOS FETs with stacked oxide-nitride and -oxynitride gate dielectrics demonstrating stress-induced interfacial defects [4]; and iii) extends new developments in constraint theory from glasses to planar device interfaces [5]. It is proposed in this paper that *transition* regions between 'rigid' and 'floppy' regions in bulk glasses serve as a *model* system for quantifying intrinsic limitations on interface abruptness in semiconductor devices with steps in average bonding coordination, as for example at Si-dielectric interfaces and at internal interfaces in stacked gate dielectrics.

This paper also addresses high-k replacement dielectrics for SiO_2, that include Al_2O_3, Ta_2O_5 and Zr(Hf) and L(Y) silicate alloys. These high-k dielectrics must eventually: i) reduce EOT to ~0.5 nm., ii) maintain device performance (e.g., drive current/unit channel length) and reliability (TDDB) at levels extrapolated from devices with SiO_2 dielectrics and Si-SiO_2 interfaces, and iii) have tunneling or gate leakage current levels below about 1-5 A/cm^2 for table top devices, and 10^{-3} A/cm^2 for portable devices. One of the most important factors in determining whether or not these three targets can be met will be the electrical quality of Si-dielectric interface, including bond-constraint induced transition regions.

2. Experimental Results

Several recent studies have addressed chemical bonding arrangements at thermally annealed Si-SiO_2 interfaces and have shown that *optimized* interfaces display transition regions ~0.3 nm thick with excess sub-oxide bonding arrangements different from those expected at abrupt Si-SiO_2 metallurgical interfaces. These studies include: i) XPS on ultra-thin Si-SiO_2 interfaces using monochromatic synchrotron radiation (see Fig. 1) [1], ii) in-situ AES [2] and iii) in-situ FTIR [3].

It is significant to note that as-grown interfaces formed by either thermal oxidation, or plasma-oxidation in Fig. 1

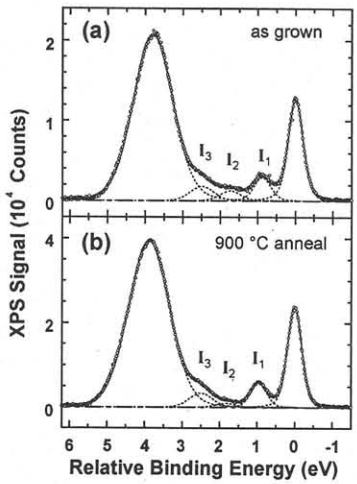

Fig. 1. Soft X-ray photoelectron spectra from Si (111) as-grown and after a 900°C anneal. Sub-oxide bonding groups are labeled I_1, I_2 and I_3 following the conventional interpretations of Ref. 1.

display significantly more suboxide bonding than after a 900°C anneal [6]. After this anneal, the relative concentrations of the different suboxide bonding arrangements in the transition regions are characteristic of the particular Si surface orientation. For example Si^{2+} arrangements, which are not 'native' on Si(111) interfaces are reduced more than the 'native' Si^{1+} and Si^{3+} arrangements.

These intrinsic transition regions will limit device performance and reliability. For example, they are more than likely the basis for the so-called universal mobility-field relationships for channel carriers as well as the u-shaped density of interface traps distributions obtained from C-V studies. For example the local charge on Si atoms in sub-oxide regions will vary with the number of O-atom neighbors, and thereby scatter channel holes and electrons.

Data from NMOS and PMOS FETs with plasma-grown Si-SiO_2 interfaces, and plasma deposited oxide, oxynitride alloy and nitride dielectrics (EOT~1.3 to 2.0 nm) have revealed relationships between performance and reliability that are correlated with bonding coordination differences at internal dielectric interfaces. Analysis of C-V data have indicated increased levels of fixed positive charge at internal SiO_2-oxynitride and SiO_2-nitride interfaces relative to internal plasma-grown SiO_2-plasma deposited SiO_2 interfaces (see Fig. 2), as well correlations between increased interfacial charge and i) decreased carrier mobility (see Fig. 3) and ii) reduced reliability. These decreases are correlated with increases in the average number of bonds/atom, N_{av}, between SiO_2-oxynitride (~2.85) and SiO_2-nitride (~3.1), where a value of $N_{av} \sim 3$
has been shown to define the boundary between 'device-quality' and 'more defective' interfaces. [7].

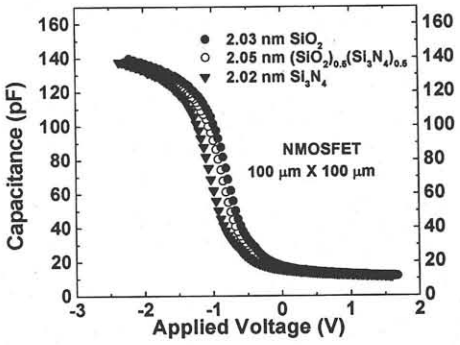

Fig. 2. C-V curves for stacked gates. Displacements are due to fixed positive charge at internal dielectric interfaces.

Fig. 2. C-V curves for stacked dielectrics with 0.6 nm SiO_2 plasma grown interfacial oxides. These data combined with data for PMOS devices indicate that the negative voltage shifts with respect to the stacked SiO_2 device derive from fixed charge at internal dielectric interfaces.

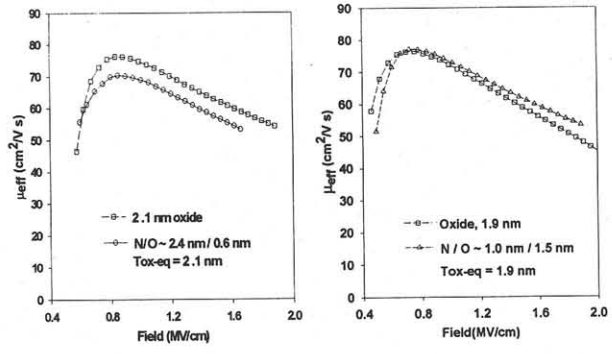

Fig. 3. Differences in mobility for the stacked devices correlate with distance of the internal dielectric interface from the Si channel region.

3. Extension of Constraint Theory to Interfaces

Applications of constraint theory to non-crystalline solids have focussed on bulk glasses [8], thin films [9] and $Si\text{-}SiO_2/Si_3N_4$ interfaces [7]. The average number of bonding constraints per atom, C_{av}, as determined by valence stretching and bending forces, is directly proportional to the average number of bonds per atom, N_{av}, through the relationship: $C_{av} = 2.4\ N_{av} - 3$. When the number of constraints/atom is equal to the network dimensionality, then good glass formation ensues as for As_2S_3. A very week bond-bending force at the O-atom sites in SiO_2 also results in C_{av} being equal to 3. Strain builds up in a glass or thin film when N_{av} exceeds a critical value of 2.4 (or 2.67 for SiO_2) that corresponds to $C_{av} = 3$. Since bending forces are weaker than stretching forces, this results in bond rupture and defect formation. Theory predicts that bond-angle strain, $\Delta\theta$, is proportional to the $N_{av} - N_{av}^*$, where N_{av}^* corresponds to an unstrained, ideal glass or film. Strain energy is proportional to $(\Delta\theta)^2$, so that the defect concentrations scale as $(N_{av} - N_{av}^*)^2$. This scaling has been demonstrated for Si-dielectric interfaces [7], and accounts for the high defect densities at $Si\text{-}Si_3N_4$ interfaces relative to $Si\text{-}SiO_2$, where the respective values of $N_{v,int}$ are 2.86 and 3.45. Constraint theory can not identify specific defect environments, other than possibly dangling bonds, and cannot predict defect densities.

Recently, both theory [5] and experiment [10] have identified a new aspect of constraint theory by demonstrating that 'rigid (or over-constrained)' and 'floppy (or under-strained)' regions in an alloy glass are separated by mono-layer interface layers that are 'over-constrained' with respect to bonding coordination. These regions are not

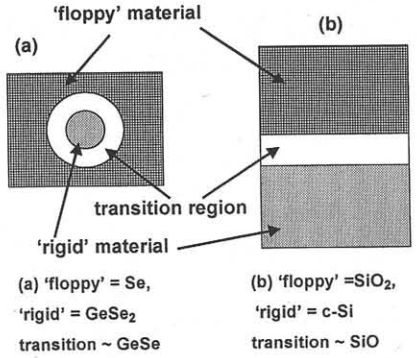

Fig. 4. Analogy between bulk glasses and films and dielectric interfaces. This schematic shows the interfacial transition regions.

'mechanically-strained'. Fig. 4 presents a schematic representation of the extension of this theory from bulk glasses and films to interfaces. Experiments cited in Refs. 1-4, combined with the theory of Refs. 5 and 11, suggest that the interfacial transition regions in advanced Si FET gate stacks are *intrinsic*, and result from entropy effects. These transition regions constitute a basic limitation for the aggressive-scaling of CMOS Si devices, as well as other semiconductor devices with similar 'steps' in interfacial bond coordination. Finally, the average number of bonds/per atom in high-k dielectrics, computed in the context of the resonating bond picture of Pauling, is generally close to SiO_2. Therefore low densities of defects at Si-high-k dielectric interfaces are possible. In addition, if interfacial nitrided oxides are required for other reasons such as suppression of interfacial reactions during film deposition, then low densities of defects at these internal dielectric interfaces between the high-k oxides and silicates will result. This prediction has been verified in stacked gate dielectrics with remote plasma process oxide and nitrided oxide interface layers and plasma-deposited Ta_2O_5 gate dielectric films.

Acknowledgments

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