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A Guideline for Accurate Two-Frequency Capacitance Measurement for Ultra-Thin Gate Oxides

Akiko Nara, Naoki Yasuda, Hideki Satake and Akira Toriumi
Advanced LSI Technology Laboratory
Research & Development Center,Toshiba Co.
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Phone/Fax:+81-(0)45-770-3689/+81-(0)45-770-3578, e-mail:nara@amc.toshiba.co.jp

Introduction

Accurate capacitance measurement has become increasingly difficult as the oxide layer thickness has been reduced below 2 nm due to an increase of the direct tunneling leakage current. Although an impedance analysis method has been proposed [1], we have found that it requires accurate measurements at frequencies higher than 1 MHz in the sub-2 nm region. A two-frequency technique has also been proposed [2], but we have found that it cannot be applied in the sub-2 nm region to randomly selected frequencies. In this paper, we propose a novel guideline for obtaining an accurate capacitance in sub-2 nm region from two-frequency C-V technique.

Limitations of the Two-frequency Technique

An equivalent circuit model of a MOS structure with an ultra-thin gate oxide must include a parasitic resistance (Rp) in parallel with the capacitance to account for the gate leakage current and a series resistance (Rs) (Fig.1 (a)). In practice, LCR meters only offer measurement models corresponding to two-parameter models, such as the one shown in Fig.1 (b). K. J. Yang et al. have proposed a technique where measurements are performed at two different frequencies [2]. The true device capacitance, C, can be extracted using eq.1 in Table.1 [2], where C_i and D_i (i=1,2) correspond to the measured capacitance and dissipation at a frequency f_i. The method poses no theoretical limits on the choice of measurement frequencies. However, we found that this technique cannot be applied to randomly selected frequencies f_i (i=1,2). Fig.2 shows the capacitance error obtained with the two-frequency technique for a MOSFET with a 1.8 nm-thick oxide. In the case of f_1=1 kHz and a variable f_2, the capacitance calculated from eq.1 varies by up to 50%. The capacitance variation drops to a few percent when f_1=1 MHz and f_2 is variable. Obtaining a frequency-independent capacitance using the two-frequency technique clearly requires additional consideration.

New guideline for ultra-thin gate oxide

Accuracy of the calculated capacitance is given by eq.2, where ε is the relative measurement error of the LCR meter. If we assume that the measured capacitance does not change appreciably over the measurement frequency range and $D_i f_i$=const. (i=1,2), eq.2 can be rewritten as shown in eq.3, where $k=f_2/f_1$. The relative error $\Delta C/C$ can be minimized by reducing k, and D_1. The effect of k can be practically eliminated by selecting f_2 significantly smaller than f_1. The higher measurement frequency, f_1, should be selected to the point where D reaches its minimum to reduce the effect of D_1. In order to satisfy the ITRS requirement of less than 4% error in T_{ox} [4], the ε multiplier in eq.3 should be less than 8. The measurement error of the LCR meter, ε, can reach 0.5%[3]. This condition is true when D_1<1.1 at higher frequency f_1.

Experimental Results

Figs.4 and 5 show the measured capacitance and dissipation values at a fixed frequency for various T_{ox}. As shown in Fig. 5, the frequency range in which the D<1.1 requirement is satisfied became very limited, and shifted to higher frequencies for the thinner oxides. Fig.6 shows the bias voltage dependence of the measured capacitance (symbols) at a single frequency and the corrected capacitance (solid lines), using the two-frequency technique proposed in this study. The selected frequencies were 2 MHz and 400 kHz for 1.8 nm oxide, and 600 kHz and 100 kHz for thicker than 2.5 nm oxide. Here, we would like to emphasize that a single frequency measurement does not provide the true capacitance for thinner than 2 nm oxides. The thickness obtained from the two-frequency C-V technique shows good agreement with the thickness obtained from high-resolution transmission electron microscopy (HRTEM) images (Fig.7), even in sub-2 nm region.

Conclusions

An improved C-V extraction guideline of ultra-thin MOS structure was proposed to overcome the limitations of the conventional two-frequency C-V technique. We have experimentally demonstrated the validity of this procedure by showing that a measurement error of less than 4% can be achieved by performing where dissipation is less than 1.1 at higher frequency.

References

[1] M. Matsumura et al., JJAP **38**, L845(1999).
[2] K. J. Yang et al., IEEE Trans. Electron. Dev., **46** 1500(1999).
[3] Hewlett Packard, model 4284 Manual (1998).
[4]ITRS, (SIA) (1999).

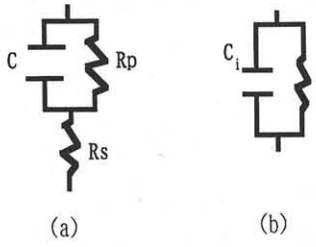

Fig. 1 Equivalent circuit models.
(a) Three-parameter model for ultra-thin film.
(b) Two-parameter model for single frequency measurement.

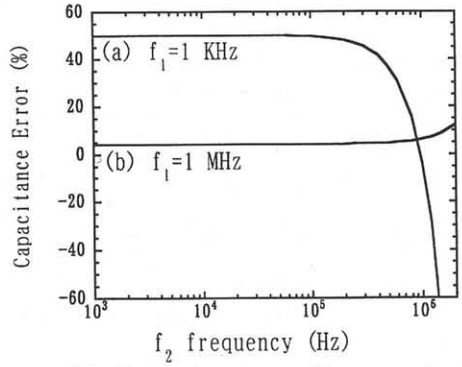

Fig. 2 Error(%) of calculated capacitance vs f_2. f_1 is 1kHz in (a) and 1MHz in (b).

Table. 1 List of equations used in the proposed technique.

$$C = \frac{f_1^2 C_1 (1+D_1^2) - f_2^2 C_2 (1+D_2^2)}{f_1^2 - f_2^2} \quad (1)$$

$$\frac{\Delta C}{C} = \varepsilon \frac{f_1^2 C_1 (1+3D_1^2) + f_2^2 C_2 (1+3D_2^2)}{f_1^2 C_1 (1+D_1^2) - f_2^2 C_2 (1+D_2^2)} \quad (2)$$

$$\frac{\Delta C}{C} = \varepsilon \frac{1+k^2+6D_1^2}{1-k^2} \quad (3)$$

$$k = \frac{f_2}{f_1}$$

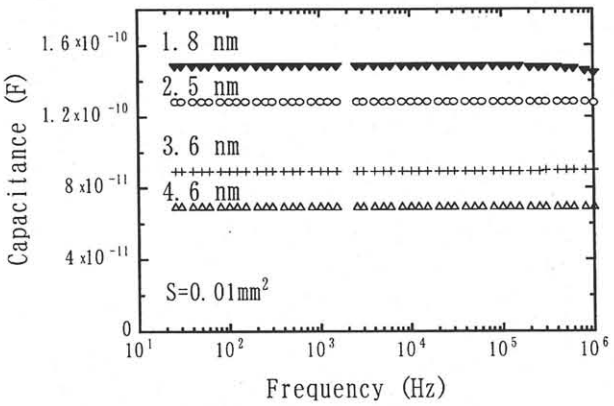

Fig. 4 Frequency dependence of capacitance for various oxide layer thicknesses at a bias of -2V.

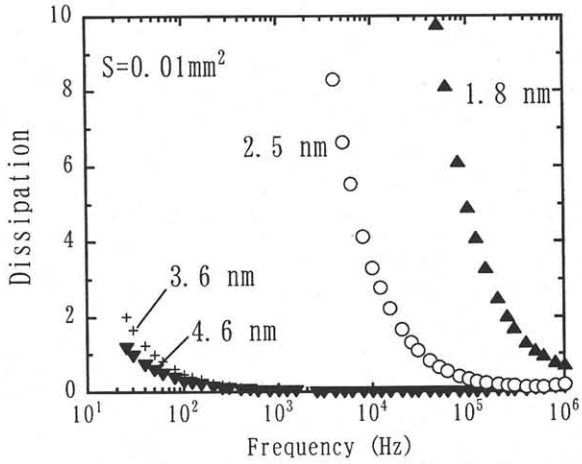

Fig. 5 Frequency dependence of dissipation values for various oxide layer thicknesses at a bias of -2V.

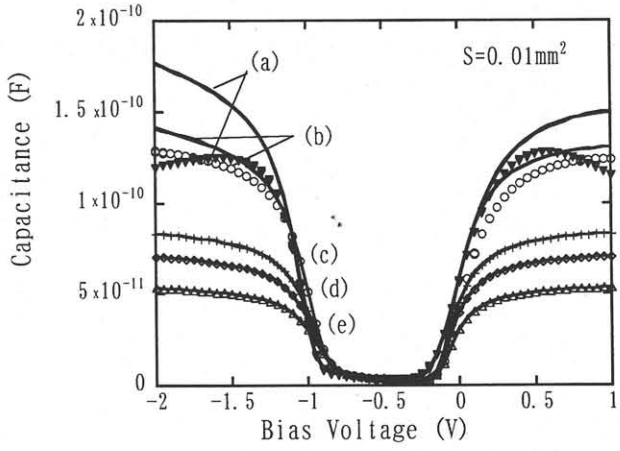

Fig. 6 C-V characteristics of nMOSFET devices with oxide layer thickness of (a) 1.8nm (b) 2.5nm (c) 3.6nm (d) 4.6nm (e) 6.2nm measured at a fixed frequency are indicated by symbols.
Calculated capacitance is indecated by continuous lines.

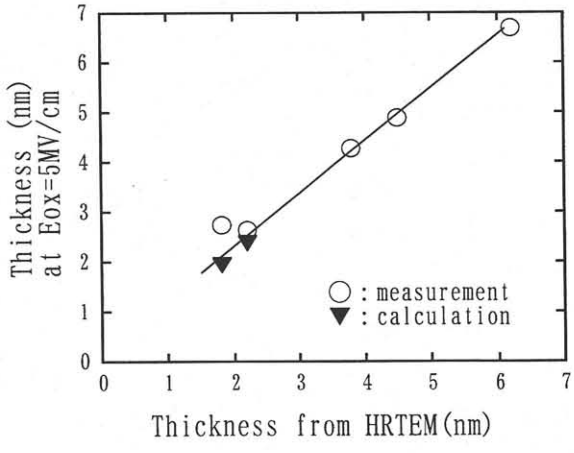

Fig. 7 Comparison of oxide thickness obtained from single-frequency measurement(○), and two-frequency calculations(▼) and HRTEM observations.