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Novel Method of Threshold Voltage Control of Metal Gate CMOSFETs Using Channel Epitaxy

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1. Introduction

For MOSFET scaling, gate oxide scaling is most challengeable. However, as the thickness of gate oxide is scaled down to below 2.5㎚, gate poly depletion increases over 10% of the total thickness and becomes a limiting factor of sub-100㎚ MOSFET scaling. To eliminate gate depletion, metal gate has been suggested. Metal gate MOSFET has no gate depletion problem. In addition, metal gate has low resistance which is suitable for the sub-100㎚ transistor with a scaled gate stack width and height. Over these advantages, even though low threshold voltage(V_{th}) is necessary for low power CMOS application, it is difficult to maintain low V_{th} with metal gate because most metals have midgap work function.

In this paper, we present the outstanding characteristics of the CMOSFETs with metal gate fabricated using damascene process [1]. To lower V_{th}, channel epitaxy after dummy gate removal was introduced. And to reduce S/D resistance, S/D elevation with SEG and silicidation were also applied.

2. Experiments

The process flow of the metal gate electrode formation is schematically shown in Fig. 1. Isolation, channel, and S/D were formed and two optional processes were applied to reduce R_{sd}. One is elevated S/D of 500Å Si using SEG. The other is Co-silicided S/D. After the formation of the transistor with dummy poly-Si gate, dummy poly-Si gate was removed. To reduce V_{th}, channel epitaxy or channel counter doping was performed. RTO was used to form gate oxide, and then (CVD TiN, PVD TiN)/W gate stacks were followed. Finally, CMP process completed metal gate formation.

3. Results and Discussion

A. High performance PMOS

Fig. 2 shows C-V curves of the MOS capacitors with poly-Si gate and metal gate. As expected, metal gate has no gate depletion, but poly-Si gate has gate depletion of ~3 Å, which is more serious especially for PMOS because boron solubility in poly-Si is lower than arsenic by about one order of magnitude. Moreover boron penetration problem in PMOS does not exist. Therefore PMOS performance using metal gate is drastically enhanced as shown in Fig. 3. I_{on}=425㎂/㎛ with pure oxide 20Å and I_{on}=445㎂/㎛ with pure oxide 13Å at V_{dd}=1.5V, I_{off}=1㎁/㎛ were obtained. Compared with I_{on}=340㎂/㎛ of poly-Si gate, it is the record of PMOSFET even with unsilicided S/D [2]. Ring oscillator delay is shown on Fig. 4.

B. Threshold voltage control

Although metal gate has no gate depletion, the V_{th} of metal gate is higher than that of poly-Si gate due to the midgap work function. Counter-doping of channel has been widely used to lower V_{th} (Fig. 5)[3], but with this method the subthreshold swing is severely degraded even for the long channel MOSFET because of buried channel formation (Fig. 6).

Undoped Si was epitaxially grown only in the channel region using SEG (Fig. 7). V_{th} was lowered by ~0.35V and good short channel characteristic was maintained compared to non-SEG MOSFET (Fig. 8 & Fig. 9). Also, it is very important to note that the subthreshold swing($\leq$93 ㎷/dec) of SEG MOSFET is not degraded because of the surface channel formation instead of the buried channel with counter doping (Fig. 10 & Fig. 11). This results present that lowering V_{th} of metal gate to the values for the conventional CMOS is possible without disadvantages of the buried channel.

The gate length of SEG MOSFET is slightly enlarged due to the convex shape of the channel surface, which may increase accumulation resistance and degrade current drivability.

C. Source/drain resistance

Low R_{sd} is inevitable for high performance MOSFETs. So elevated S/D were formed using SEG in Fig. 12. With elevated S/D, I_{on} was increased due to reduction of R_{sd} by 15%. With the Co-silicidation of S/D region (Fig. 13), R_{sd} is reduced by 33% (Fig. 14).

D. Reliability

Reliability is another issue on metal gate in terms of metal ion diffusion into gate oxide and plasma damage during the metal etching process. Damascene gate minimizes plasma damage due to etching free process. CVD TiN gate has good TDDB characteristics, guaranteeing 10-year lifetime at room temperature (Fig. 15), even though, it still needs to be improved.

4. Conclusion

High performance CVD TiN/W metal gate CMOSEFTs were fabricated by damascene process. For PMOS, I_{on}=445㎂/㎛ was achieved at I_{off}=1㎁/㎛, V_{dd}=1.5V. Elevated channel epitaxy was introduced, which enabled us to lower V_{th} to the values of poly-Si gate MOSFET. Contrary to the MOSFET with buried channel, the MOSFET using channel epitaxy shows surface channel characteristics without subthreshold swing degradation. The R_{sd} of silicided S/D was reduced by 33%.

References

[1] A. Yagishita et al., *IEDM Tech. Dig.*, p. 785, 1998
[2] M. Mehrotra et al., *IEDM Tech. Dig.*, p. 419, 1999
[3] A. Chatterjee et al., *IEDM Tech. Dig.*, p. 821, 1997

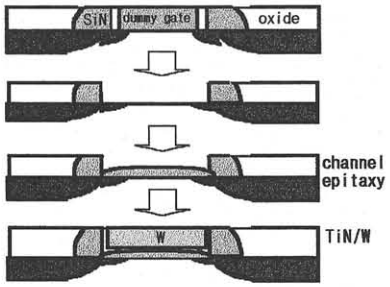

Fig. 1 Schematic diagrams of damascene metal gate process with channel epitaxy.

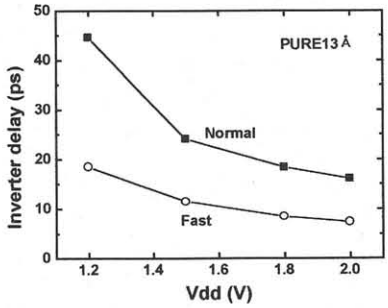

Fig. 4 Inveter delay of 51-stage ring oscillator versus V_{dd}.

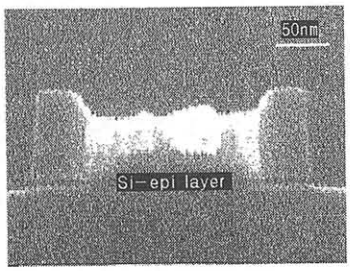

Fig. 7 SEM image of a MOSFET with elevated channel and metal gate.

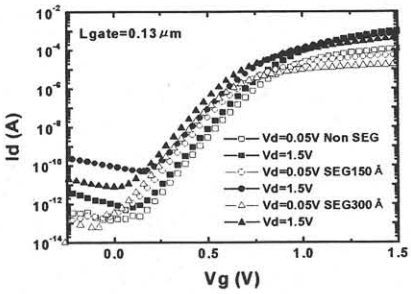

Fig. 10 I_d versus V_g of NMOSFETs with elevated channel by SEG.

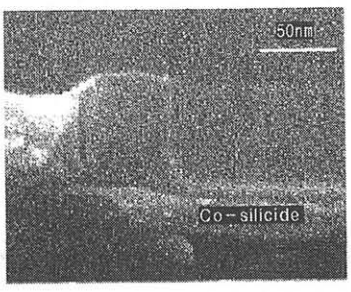

Fig. 13 SEM image of a MOSFET with Co-silicided S/D.

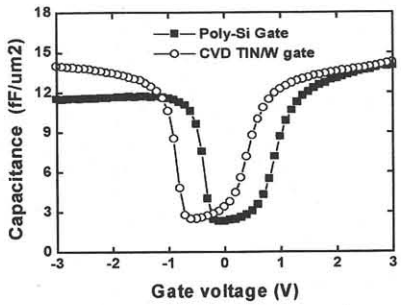

Fig. 2 C-V curves of PMOS capacitors with TiN/W gate and poly-Si gate

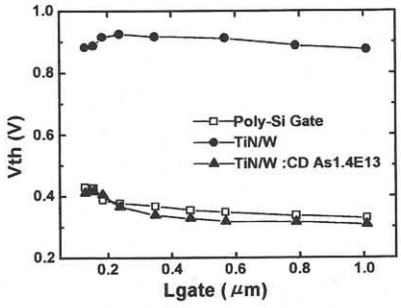

Fig. 5 V_{th} versus gate length of NMOSFETs with poly-Si gate, metal gate, and metal gate with counter-doping.

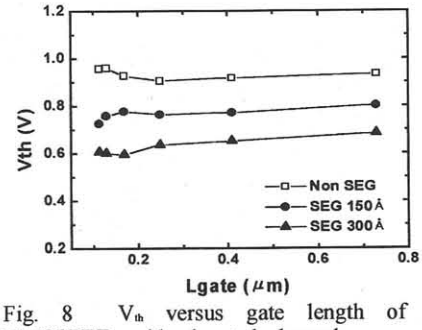

Fig. 8 V_{th} versus gate length of NMOSFETs with elevated channel

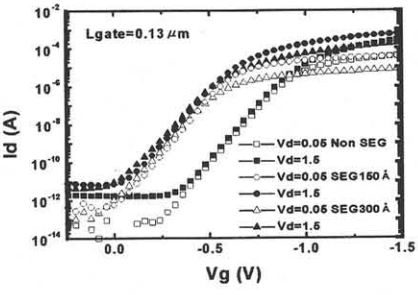

Fig. 11 I_d vs V_g of PMOSFETs with elevated channel by SEG.

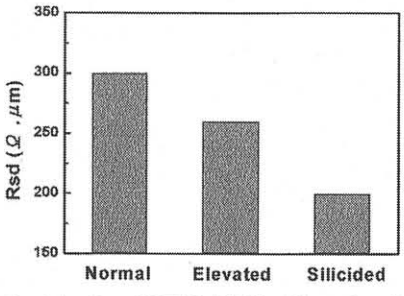

Fig. 14 R_{sd} of NMOSFETs. Normal refers to-non elevated and non-silicided S/D.

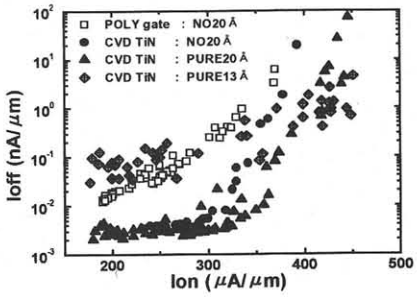

Fig. 3 I_{off} versus I_{on} of PMOSFETs with various gate electrodes. V_{dd}=1.5V.

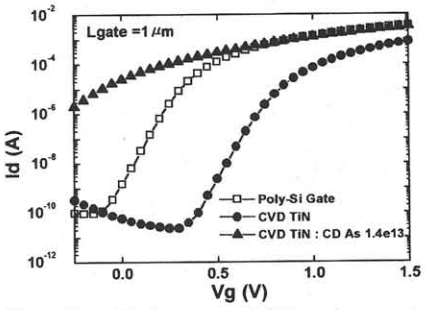

Fig. 6 Drain currents(I_d) versus gate voltage(V_g) of NMOSFETs. Metal gate with channel counter-doping degrades subthreshold swing.

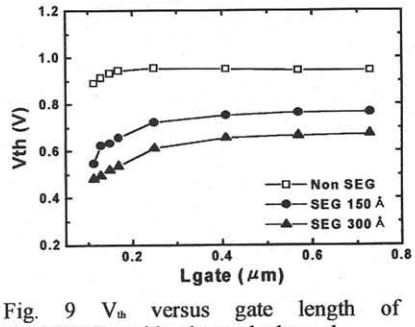

Fig. 9 V_{th} versus gate length of PMOSFETs with elevated channel

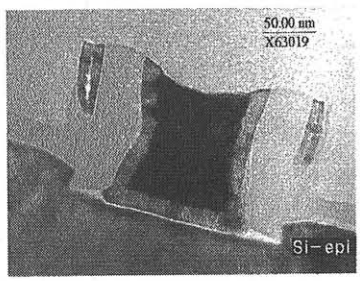

Fig. 12 TEM image of a MOSFET with elevated S/D by SEG.

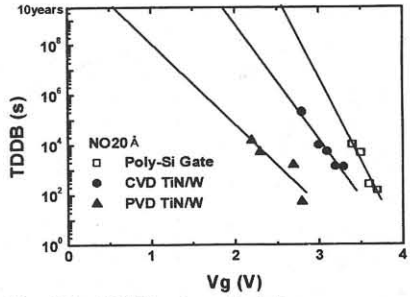

Fig. 15 TDDB characteristics.