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Low Resistivity PVD TaNx/Ta/TaNx Stacked Metal Gate CMOS Technology Using Self-Grown *bcc*-Phased Tantalum on TaNx Buffer Layer

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Abstract

We have developed low-resistivity (~15μΩcm) *bcc*-phased tantalum gate CMOS technology having Tantalum Nitride (TaNx) buffer layer. TaNx works not only as a buffer layer which prevents the reaction between metal tantalum film and gate oxide film, but also as a seed layer which helps self-growth of *bcc*-phased tantalum film by hetero-epitaxy.

In this paper, we demonstrate excellent characteristics of Fully-Depleted Silicon-On-Insulator(FDSOI) CMOS devices using TaNx/*bcc*-Ta/TaNx stacked metal gate structure.

Introduction

As CMOS devices are scaled down aggressively, metal gate technology has become important, because of their low-resistivity and no gate depletion unlike polysilicon.

Moreover it is attractive for FDSOI devices due to near midgap work function[1].

Recently, metal gate devices having W/TiNx stacked gate (using conventional plane gate structure) have been reported [2-4], but there exists a severe difficulty that TiNx and W films are dissolved in acid solution during cleaning steps. On the other hand, both Ta and TaNx films have high durability to wet chemical cleanings. Besides capped TaNx layer is introduced as a protect layer from oxidizing ambience, TaNx layer has already been confirmed to serve as a very promising diffusion barrier of the diffusive copper[5].

In this work, we have found for the first time that low-resistivity *bcc*-tantalum layer is stably self-grown on TaNx buffer layer due to hetero-epitaxy by sputtering even if ion energy is maintained at low levels such as 10 eV [6].

Excellent characteristics of MOS capacitors on bulk and FDSOI-CMOS devices using TaNx/*bcc*-Ta/TaNx stacked metal gate are demonstrated.

Experimental

TaNx(15nm)/*bcc*-Ta(160nm)/TaNx(5nm) stacked gate (Rs ~1.0Ω/sq.) was formed sequentially by sputtering at room temperature without breaking the vacuum to suppress Ta surface oxidation. Xe gas for Ta and ($Xe+N_2$) mixed gas for TaNx were used respectively to suppress plasma induced damages to gate oxide[7]. MOS capacitors on bulk substrate and FDSOI-CMOS FETs on SOI (57nm) were fabricated with the stacked metal gate structure (Fig.1). Gate oxides (11.5nm for capacitors and 3.8 or 5.5nm for FDSOI-CMOS) were grown in dry O_2 ambient at 900°C. Source/Drain of FDSOI-CMOS was formed by Ion-Implantation ($^{75}As^+$ for NMOS, $^{49}BF_2^+$ for PMOS 15KeV-1.5E15cm^{-2} respectively) and annealing below 550°C to activate implanted region without deteriorating the metal gate[8].

Results and Discussion

The effect of TaNx buffer layer on crystallographic properties is shown in Fig.2. XRD spectrum of Ta/TaNx only indicates 100% *bcc*-phase tantalum film. Contrary, spectrum of Ta/SiO_2 indicates almost high-resistivity (~160μΩcm) β-tantalum phase. It is speculated that the tantalum layer has been affected by lattice structure of under layer i.e. hetero-epitaxy. Mismatch between Ta_2N(101) and *bcc*-Ta(110) is only 0.68% (See Table 1). Evidence of this speculation for almost the same lattice constant of both layers has been demonstrated in TEM photograph (Fig.3).

Fig.4 shows interface trap density (Dit) of fabricated capacitors as a function of N_2 mixture ratio [=N_2/($Xe+N_2$)] during TaNx buffer layer sputtering. When N_2 mixture ratio is 1.0%, Dit indicates the minimum value. Fig.5 compares quasi-static C-V curves between no buffer and 1.0% TaNx buffer layer samples. Figs. 3 and 5 suggest that 1.0% TaNx buffer layer prevents the reaction between the metal tantalum film and gate oxide film. Fig.6 shows Fowler-Nordheim plots of the capacitors. This excellent linearity up to 10 orders means low leakage current except for F-N current. The barrier heights at Metal/SiO_2 interface obtained from the slopes as a function of N_2 mixture ratio are shown in Fig.7. This means that work function of TaNx gate is higher than that of β-Ta gate. Fig.8 presents gate-injected charge-to-breakdown (Qbd) characteristics of the capacitors. All samples have almost the same value despite of the difference in barrier height[9]. These results suggest that the gate oxide reliability is improved by an insertion of TaNx layer.

Fig. 9 shows Vth roll-off of fabricated FDSOI-CMOS with 1.0%TaNx buffer layer. It is also confirmed that TaNx gate indicates nearer midgap work function than β-Ta gate. Typical Ids-Vgs and Ids-Vds characteristics of the FDSOI-CMOS devices are demonstrated in Figs.10 and 11. The subthreshold slopes of 65.7/67.6 mV/decade for NMOS /PMOS (@L=0.35um) respectively have been achieved with 3.8nm thickness gate oxide. The propagation delay in the inverter are also shown in Fig.12.

Conclusion

We succeeded in fabricating TaNx/*bcc*-Ta/TaNx stacked metal gate FDSOI-CMOS devices. It is confirmed that low-resistivity *bcc*-Ta layer is stably self-grown on TaNx buffer layer by hetero-epitaxy. Furthermore, TaNx gate indicates lower Dit and nearer midgap work function than β-Ta gate.

References

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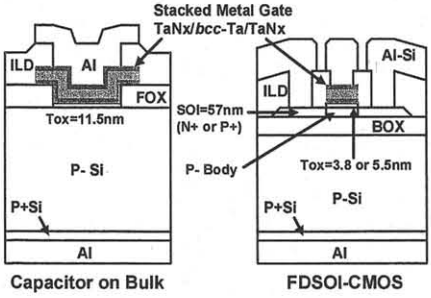

Fig. 1 Cross sectional view of fabricated capacitors and FD-SOI CMOS FETs with TaNx/*bcc*-Ta/TaNx stacked metal gate.

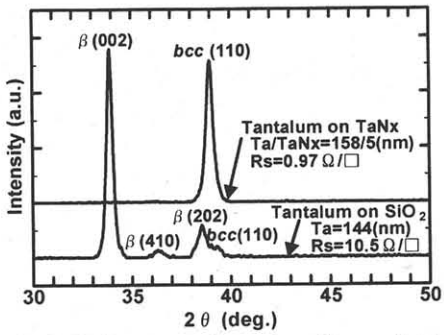

Fig. 2 XRD spectra of tantalum film on TaNx buffer layer and tantalum film on SiO_2. These samples have no TaNx cap for XRD measurement.

Table 1

Orientation, lattice constant and 2θ(Cu-Kα) diffraction data from JCPDS. Mismatch between Ta_2N(101) and *bcc*-Ta(110) [observed in Fig.2] is only 0.68%.

	(hkl)	d (nm)	2θ (deg)
β -Ta	(002)	0.2658	33.69
β -Ta	(410)	0.2474	36.28
β -Ta	(202)	0.2354	38.20
bcc-Ta	(110)	*0.2338*	*38.47*
Ta_2N	(101)	*0.2323*	*38.73*
TaN	(200)	0.2169	41.60

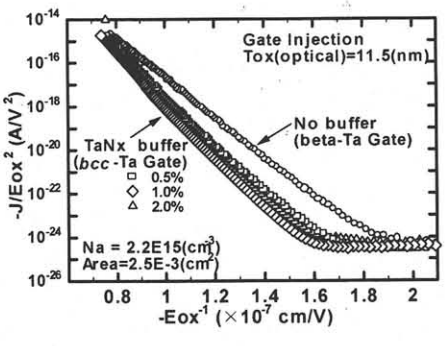

Fig. 6 F-N plots of fabricated TaNx gate MOS capacitors at Metal/SiO_2 interface.

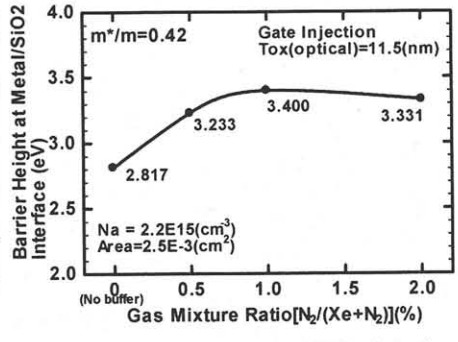

Fig.7 Barrier height at Metal/SiO_2 interface from the slopes of Fig.6. m*/m is fixed at 0.42.

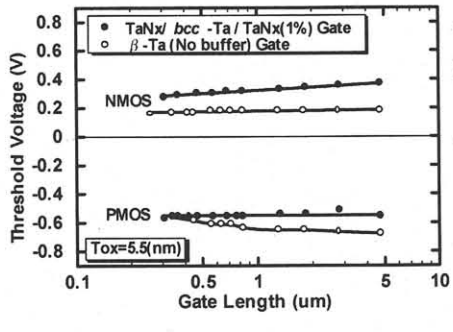

Fig. 9 Vth versus Lg for TaNx/*bcc*-Ta/TaNx (1.0%) gate and β-Ta (No buffer) gate FDSOI-CMOS FETs. Vth is measured at Vd=±0.05V.

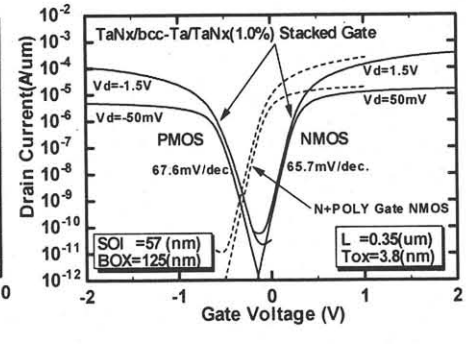

Fig.10 Subthreshold characteristics for TaNx /*bcc*-Ta/TaNx (1.0%) gate FD-SOI CMOS FETs. Characteristic of conventional N+ Poly gate NMOS is also shown.

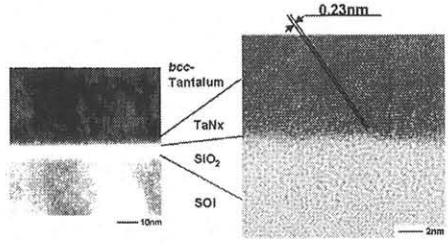

Fig. 3 Cross sectional TEM photograph of *bcc*-Ta/TaNx stacked metal gate. Lattice constant of both *bcc*-Ta and TaNx is ~0.23nm. The reaction between TaNx and SiO_2 is not observed after S/D annealing.

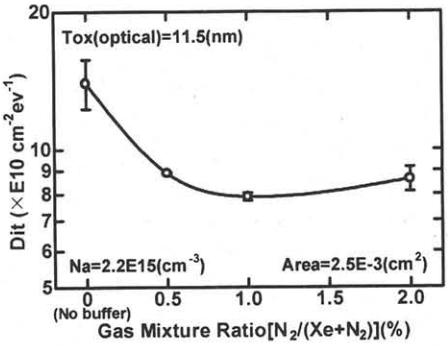

Fig. 4 Interface trap density of Si–SiO_2 interface at midgap as a function of nitrogen ratio during TaNx buffer layer sputtering.

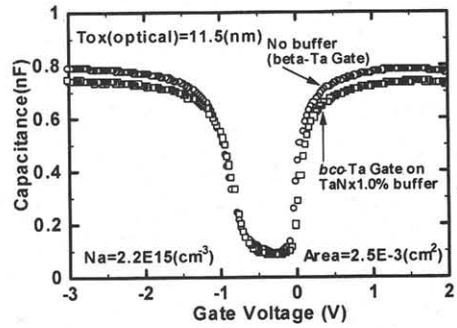

Fig. 5 Quasi-static C-V curves of *bcc*-Ta and β-Ta. The difference is due to the reaction of β-Ta with SiO_2. Cinv/Cacc of both curves are approximately 1.0.

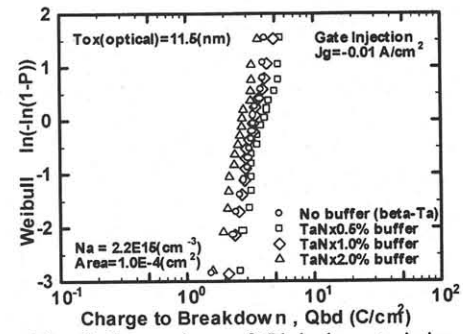

Fig. 8 Comparison of Qbd characteristics among TaNx gate MOS capacitors.

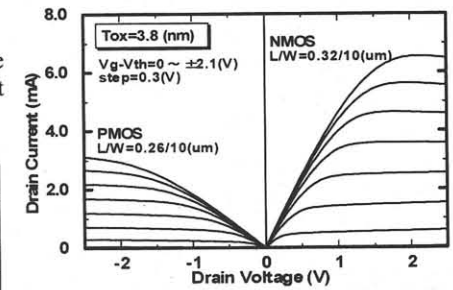

Fig.11 I_{DS}-V_{DS} characteristics of TaNx/*bcc*-Ta/TaNx stacked metal gate FD-SOI CMOS.

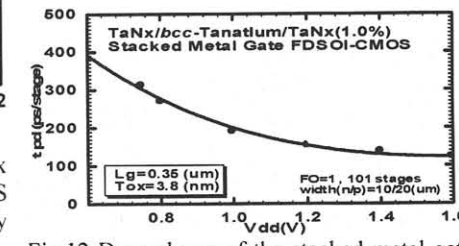

Fig.12 Dependence of the stacked metal gate FDSOI-CMOS inverter delay time on V_{DD}.