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The Role of Domains in Long Term Reliability

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1. Introduction

Imprint springs from a fundamental property of ferroelectric materials and is driven primarily by domains within the material. Understanding the impact of domains within a ferroelectric material is crucial to controlling the long term reliability of commercial devices made from these same materials. The author will discuss the role that domains play in the imprint mechanism. He will propose a relationship between voltage offsets and measured polarization. Finally, published imprint test techniques will be critiqued for accuracy relative the domain model of imprint.

2. Domains and Imprint:

The problem of imprint was first noted by Dr. Norm Abt of National Semiconductor Corporation at the International Symposium on Integrated Ferroelectrics in 1991.[1] It eventually came to be understood as retention failure of a ferroelectric memory bit as a function of the length of time that bit had previously remained in the opposite state. Imprint has become the primary reliability limitation of ferroelectric memories.

Subsequent research by Radiant Technologies, Inc. and Sandia National Laboratories, both in Albuquerque, NM, USA, has shown conclusively that domains are the driving force behind the direction of imprint and that free charges within the material are the source of the internal space charge.[2] The residual electric field of the domains causes drift of free charges within the material, producing an asymmetrical distribution of the charges. The asymmetrical distribution of charges, once trapped out into material sites, becomes a built in electric field that shifts the coercive voltages of the individual domains. Many questions still remain. What are the source(s) of the free charge? What material traps exist within the material and what are their energy levels? How much free charge exists in the material?

A second consequence of imprint is the loss of polarization produced by the capacitor. Are these two effects independent of each other or is one the consequence of the other? I propose a model below which specifies that polarization loss during imprint is a parameter dependent upon the hysteresis offset and its rate of offset.

3. Measuring Imprint

There are essentially two methods for tracking imprint, one based on hysteresis drift[3] and the other based on polarization loss[4]. Variances in these approaches also exist[5] but they measure the same parameters. In the most basic test format, the sample is set into a known polarization state. It is subjected to a high temperature and then tested for the specific parameter being studied.

Evans, et al [3] published data in 1995 that showed the relationship between polarization loss and hysteresis offset. The data was taken using the basic test format described above and it very clearly shows the relationship between polarization loss and hysteresis voltage offset.

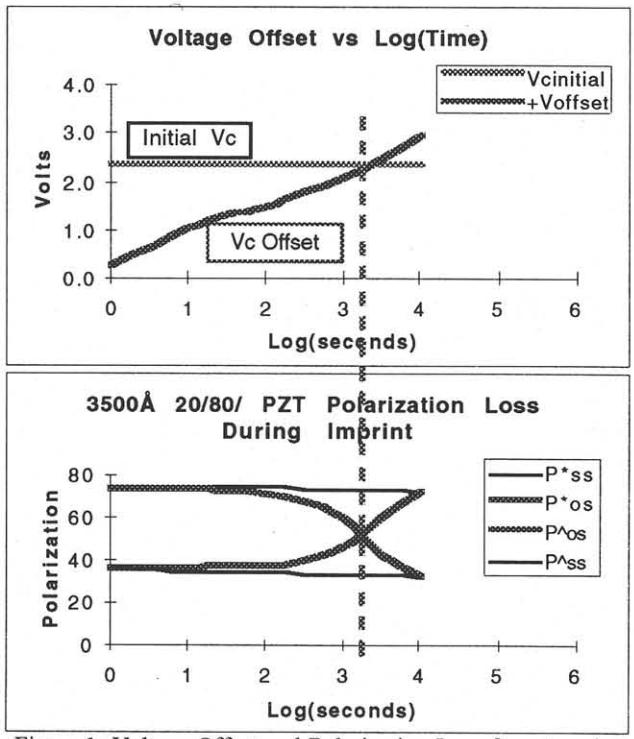

Figure 1: Voltage Offset and Polarization Loss from Imprint

The polarization failure occurs to the opposite state from that being stressed at temperature. The high and low polarization states actually reverse their positions at the point of memory failure. The other noteworthy point of interest in Figure 1 is the fact that the magnitude of the hysteresis offset voltage equals the initial coercive voltage at the point of failure. When polarization is used as the quality factor, it can only be quantified as a single number: the time to failure. And, the test must be run almost all the way to failure to be sure. On the other hand, the voltage offset parameter can be described with a linear slope. The slope can be projected to the value of the initial coercive voltage in order to predict the point of failure. The test does not have to be run to the point of

failure to accurately predict the time to failure. This is especially important when the imprint quality of the ferroelectric material is high. Such is the case for niobium doped Lead Zirconate Titanate (PNZT). The composition in Figure 1 is 0/20/80. The addition of 4% niobium as a dopant reduces the imprint rate such that it can meet a 10 year industrial specification as shown in Figure 2.

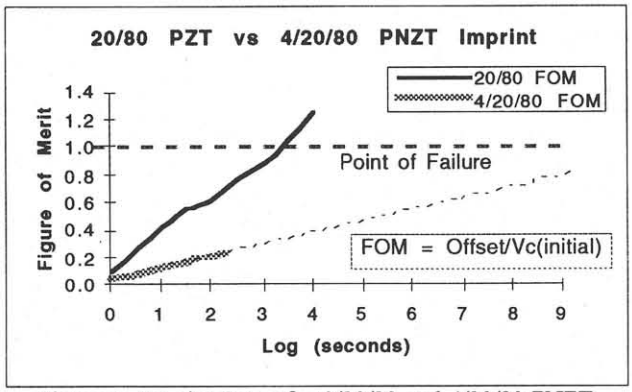

Figure 2: Imprint Rates for 0/20/80 and 4/20/80 PNZT

4. Polarization vs Voltage Offset

How then are the polarization loss and voltage offset related? The answer most likely lies in the part of the hysteresis loop associated with the remanent polarization alone. This can be measured by subtracting switching and non-switching hysteresis loops in an analogue to the pulse results of the PUND test. The Pr value in Figure 3 is the remanent polarization loop and it has its own ±Vc.

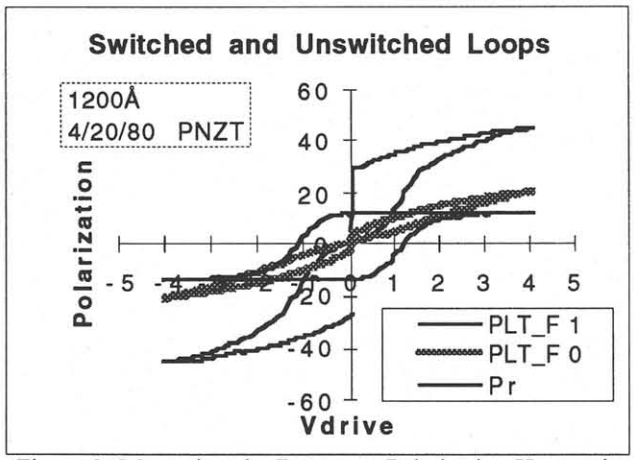

Figure 3: Measuring the Remanent Polarization Hysteresis

The shift of this loop originating from the growth of the internal field, as modeled in Figure 4, causes the loss of polarization compared to the unshifted loop. The loop in Figure 4 has been shifted to the failure point.

The two arrows represent the switched polarizations that would be measured by a PUND test. The longer one represents the polarization that would be seen at zero imprint offset. The shorter arrow represents the polarization at imprint failure. The envelope of the remanent polarization hysteresis curve is the path followed by the remanent polarization as the offset voltage grows.

The change of the remanent polarization in time can be modeled by the translation of the remanent hysteresis loop at the rate of growth of the voltage offset.

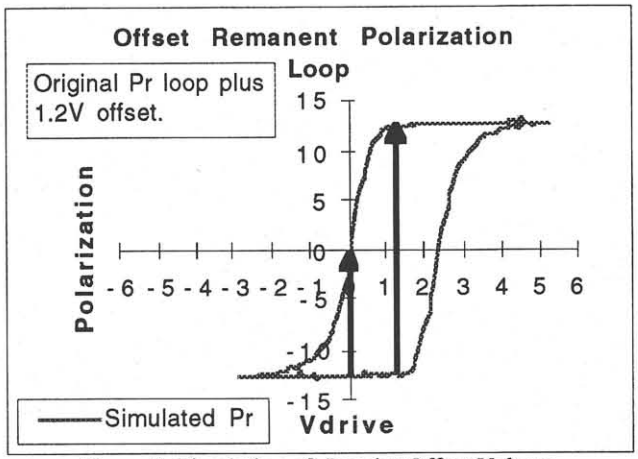

Figure 4: Simulation of Imprint Offset Voltage.

5. Test Quality

Three approaches to imprint testing have been proposed in the literature.[3,4,5] The Ramtron Q123 test [4] has been used extensively to characterize FeRAM bit failure rates, making projections based on the traditional activation energy model. This is fundamentally a polarization imprint test. Whether the test accurately predicts the true long term failure rate is dependent upon whether there is a relationship between activation energy used to characterize the bit failure rate and the imprint rate of the hysteresis voltage offset growth rate.

The static hysteresis test measures hysteresis offset voltage and can be correlated in theory with the domain model. But, it depends upon long period voltage applications to make its measurements and this condition has been shown to disturb the imprint state of the device under test [6,7]. The DC biases do not correlate with the environment of the FeRAM memory bit.

6. Conclusion

Direct measurement of the remanent hysteresis offset voltage growth rate provides the most direct measure and prediction of time to failure for a population of devices.

References

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