Nonvolatile Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS)-FETs Using Pt/SrBi$_2$Ta$_2$O$_9$/Pt/SrTa$_2$O$_6$/SiON/Si Structures Operating at 3.5V

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1. Introduction

Recently, ferroelectric-gate FETs [1,2] have attracted much attention for nonvolatile memory applications because one-transistor-cell type ferroelectric memories can be obtained and non-destructive readout operation is possible in ferroelectric-gate FETs. We have previously reported metal-ferroelectric-metal-insulator-semiconductor (MFMIS)-FETs using ferroelectric SrBi$_2$Ta$_2$O$_9$ film and SrTa$_2$O$_6$(STA)/SiON stacked buffer layer [3]. We have also shown the data retention characteristics are significantly improved when a small ferroelectric capacitor is fabricated on the large floating-gate. However, the operation voltage of the reported MFMIS-FETs was in the range of 8-10 V, which is too large for practical applications. Ferroelectric-gate FETs in other reports also need relatively high operation voltages [4-6].

In this paper, we demonstrate nonvolatile memory operation of Pt/SrBi$_2$Ta$_2$O$_9$/Pt/STA/SiON/Si MFMIS-FETs operating at ±3.5V. In particular, the effects of the area ratio $S_{MS}/S_{MFM}$, where $S_{MS}$ and $S_{MFM}$ mean the MIS and MFM areas, on the electrical properties of MFMIS-FETs are discussed.

2. Sample Preparation

P-channel MFMIS-FETs were fabricated using ferroelectric SBT and STA/SiON insulating (“I”) layers. First, field oxide regions were formed in n-(100) Si substrates for device isolation. Then, source and drain regions were formed by BF$_3^-$ ion implantation followed by the activation annealing at 1000 °C for 30 min. Next, MFMIS structures were fabricated as follows; after SiO$_2$ of the device region was removed, nitridation of the Si wafers were performed at 1050 °C for 5s in NH, ambient to form SiON layer. Then, 20-30 nm STA was formed by the sol-gel technique. The crystallization of STA was carried out at 900 °C. Measured relative dielectric constant of STA film is 110-130. SiO$_2$ equivalent thickness of STA/SiON stacked “I” layer used in this work is estimated to be 4 nm. Next, a Pt floating gate (60nm) was vacuum-evaporated and patterned by the lift-off process. Next, ferroelectric SBT films were grown by the sol-gel technique on Pt/STA/SiON/Si structures. The thickness of the SBT layer used in this work is 250 nm, which is thinner than that (400 nm) in our previous work [3]. The crystallization of SBT films was carried out by the face-to-face annealing technique at 750 °C [7]. Next, Pt gate electrodes were vacuum-evaporated and patterned. Finally, contact holes for source and drain regions were opened by the reactive ion etching (RIE) and Al electrodes were formed. The schematic cross section of the fabricated MFMIS-FETs is shown in Fig.1. Note that in the fabricated MFMIS-FETs, the area of the Pt floating gate is larger than that of the top electrodes. The area ratio $S_{MIS}/S_{MFM}$ was varied from 1 to 15. The channel length and width were 5 μm and 50 μm, respectively.

3 Results and Discussion

Figure 2 shows P-E characteristics of a Pt/SBT/Pt capacitor which is simultaneously fabricated with the MFMIS-FETs. Excellent ferroelectric properties are obtained by the face-to-face annealing method. Remanent polarization 2P, and coercive filed $E_c$ are 20 μC/cm$^2$ and 41 kV/cm, respectively.

Figure 3 shows typical drain current - gate voltage ($I_D$-V$_G$) characteristics of fabricated Pt/SBT/Pt/STA/SiON/Si MFMIS-FETs at drain voltage of -0.1 V with a gate voltage sweep of ±3.5V. The area ratio $S_{MIS}/S_{MFM}$ is varied from 3 to 15. It is found that the memory window is only 0.5V for the device with $S_{MIS}/S_{MFM}$=3, which indicates that only one of the minor P-E loops is used. On the other hand, when the area ratio $S_{MIS}/S_{MFM}$ is larger than 9, the memory window is almost constant and as large as 1.5 V, which shows the saturated P-E hysteresis loop is effectively used in the devices with such area ratios. Even if the gate voltage sweep is reduced to ±1.5V, MFMIS-FETs with $S_{MIS}/S_{MFM}$=15 has a memory window of 1.0V. Hence, by increasing the area ratio $S_{MIS}/S_{MFM}$ and reducing the SBT thickness to 250 nm, the MFMIS-FETs operating less than 3.5V is successfully fabricated. The gate leakage current is less than 3x10$^{-8}$ A/cm$^2$ at a gate voltage of ±3.5V.

Next, we examine the data retention characteristics. Figure 4 shows on and off drain currents of MFMIS-FETs with area ratios $S_{MIS}/S_{MFM}$ of 6, 9, and 15. To measure data retention characteristics, we first applied a ±3.5V programing pulse to write “1” or “0”, then the gate voltage was maintained at 0.35 V during a certain retention time, and the drain current was measured at a drain voltage of -0.1 V. It is
found that the data retention characteristics can be improved by increasing the area ratio. When the area ratio is 15, on and off drain current ratio is still 3 orders of magnitude after 11 hours have passed, even if the programming pulse is as low as ±3.5V.

4. Summary
Non-volatile memory operations of p-channel MFMIS-FETs operating less than 3.5V have been demonstrated using Pt/SBT/Pt/STA/SiON/Si structures. A memory window of 1.5V was obtained for the device with an area ratio $S_{MS}/S_{MFM}=15$, even if the gate voltage sweep is as small as ±3.5V. It was found that the data retention characteristics was also improved by reducing the MFM capacitor area.

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References

Fig.1 Schematic cross section of the fabricated MFMIS-FET.

Fig.2 P-E characteristics of the SBT film used for MFMIS-FETs

Fig.3 $I_D-V_G$ characteristics of Pt/SBT/Pt/STA/SiON/Si MFMIS-FETs

Fig.4 Drain currents of MFMIS-FETs as a function of the data retention time. The area ratios $S_{MS}/S_{MFM}$ of the measured devices are 6, 9, and 15