Studies on Improving Retention Time of Memorized State of MFIS Structure for Ferroelectric Gate FET Memory

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1. Introduction
There exists a great interest in the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) FET as a nonvolatile memory device. The FET-type memory is more feasible due to its nondestructive readout capability and compliance with the scaling rule, than the storage capacitor-type. However, the MFIS FET has difficulties in realizing sufficiently long retention time of memorized state. It is mainly because of depolarization field which intrinsically exists in the stacked-gate structures.

In this study, we have analyzed the retention characteristics regarding the effect of leakage current in the ferroelectric and the insulator layers by our newly developed simulation.

2. Analysis
Band diagrams of an MFIS structure with no bias voltage are shown in Fig.1. Even when bias voltage is not applied to the MFIS structure, electric field exists in the ferroelectric and the insulator layers. Therefore, current flows through the ferroelectric and the insulator films under the electric field. In order to investigate the origin of the retention characteristics of MFIS structure, we derived equations (1)-(4) as follows,

\[ D = \varepsilon_0 \varepsilon_r E_r + P_a, \]

\[ E_r = \frac{-Q_0 - Q_i}{\varepsilon_0 \varepsilon_r}, \quad E_i = \frac{-Q_i}{\varepsilon_i}, \]

\[ -dQ_w/dt = J_i(E_r) - J_l(E_i), \]

where \( D \): electric displacement in the ferroelectric layer, \( E_r \): electric field in the ferroelectric, \( \varepsilon_r \): permittivity of free space, \( P_a \): contribution to the polarization due to switching dipoles and simulated by Miller’s equation[1], \( Q_w \): injected charge density into the interfacial region of the ferroelectric and the insulator, \( Q_i \): surface charge density of the semiconductor, \( \varepsilon_i \): dielectric constant of the insulator, \( V_g \): voltage applied to the MFIS, \( d \): thickness of the ferroelectric and the insulator, \( V_0 \): surface potential of the semiconductor, \( V_{\text{flat}} \): flat-band voltage, \( J_i \) and \( J_l \): leakage current densities in the ferroelectric and the insulator, respectively.

\[ J_l = J_{0} t^{-\beta}, \]

where \( \beta \) of 0.52 was experimentally obtained in the film. So, the current density can be simulated by the product of modeled curve of Fig.2(a) and Eq. (5).

3. Results and Discussion
The MFIS structure is polarized on write operation and then is short-circuited on hold operation. Initial state of the hold operation have to be determined to simulate retention charac-
teristics. If \( J_i \) and \( Q_{\text{init}} \) are assumed to be 0 initially, the state of the MFIS structure is determined definitely by \( V_m \) and \( P_d \). So the initial state of the hold operation is determined by the initial ferroelectric polarization \( P_{\text{dini}} \), which is a value of \( P_d \) right after the write operation.

Ageing effect of ON and OFF capacitances has calculated by solving Eqs.(1)-(5) for Al/SBT/SiO\(_2\)/Si structure. The calculated capacitances are drawn by a dashed line for \( \Delta \Phi_0 = 0 \) eV, and agreed well with the measured data (solid line) [2]. This agreement supports the validity of our model. Retention time is defined as the time when the capacitance difference between ON and OFF state decays to a half of the initial value (Fig.3).

Figure 4(a) shows \( d_m \) dependence of retention time and \( P_{\text{dini}} \) at \( V_m = V_g \) of -0.35 V. Retention time drastically increases as the \( d_m \) decreases. There are mainly two reasons to explain this phenomenon. One is the increase of \( P_{\text{dini}} \) and the other is decrease of \( J_i \) at the hold state. \( P_{\text{dini}} \) increases with decreasing \( d_m \) as shown in Fig.4(a). The increase of retention time is induced by increase of \( E_r \) at the write operation and decrease of \( E_r \) at the hold operation. However, dependence of the \( P_{\text{dini}} \) decreases with \( d_m \) more slowly than retention time. This fact indicates that decrease of \( J_i \) effectively affects the increase of the retention time.

On the other hand, when \( d_m \) is reduced, electric field in the SiO\(_2\) layer at the hold state increases. However, this field at the initial hold state is only 1.73 MV/cm, even if \( d_m \) is 1 nm. Therefore, we can neglect tunneling current though SiO\(_2\) layer.

Figure 4(b) shows \( d_m \) dependence of retention time for different thicknesses of SiO\(_2\). As \( d_m \) increases, \( E_r \) at both write and hold operations decreases. Therefore, there exists an optimum value of \( d_m \). The optimum \( d_m \) increases with increasing \( d_m \). Actually, the optimum \( d_m \) is 1.1 \( \mu \)m even when \( d_m \) is as thin as 3 nm.

In order to improve the retention characteristics of MFIS structures, we focused on the effect of an increase of barrier height between the metal and the ferroelectric \( (\Delta \Phi_h) \). The parameter \( \Phi_h \) was obtained from experimental data. Figure 3 also suggests that the larger \( \Delta \Phi_h \) is quite effective to improve the retention time. The calculation shows that \( \Delta \Phi_h = 0.12 \) eV is required to realize several years of the retention time.

4. Conclusion

The retention characteristics for MFIS structures have been examined using our new simulation method which considers leakage current through the ferroelectric and the insulator layers. The calculated curves agree well with the experimental data. We found that the barrier height between the top electrode metal and the ferroelectric film is quite essential to control the retention time. Therefore, an increase in the barrier height is very effective to improve the retention time.

References