Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 274-275

C-4-6

Electrical Characteristics of $Pt/SrBi_2Ta_2O_9/Ta_2O_5/Si$ Using Ta_2O_5 as the Buffer Layer

Hoon Sang Choi[1,2], Kun Sang Park[1], Yong Tae Kim[2] and In-Hoon Choi[1]

[1]Department of Materials Science and Engineering, Korea University, Sungbukgu, Seoul 136-701, Korea
Phone: +82-2-928-8466 Fax: +82-2-928-8466 e-mail: choihoonsang@hanmail.net
[2]Semiconductor Device Lab., Korea Institute of Science and Technology,
P.O.Box 131, Cheongryang, Seoul 130-650, Korea

1. Introduction

In recent years, there has been a lot of interest in the development of non-volatile memories based on ferroelectric materials [1]. Ferroelectric based gate insulator field effect transistors are extremely important in the development of nondestructive read-out (NDRO) nonvolatile memories [2,3]. For the NDRO-FRAMs, a ferroelectric gate structure is required but it is still difficult to obtain a good quality ferroelectric thin film on the Si surface and reduce the interface trap density between the ferroelectric thin film and the Si [4,5]. Whenever oxide based ferroelectric film is deposited on Si, a thin layer of SiO_2 develops at the interface during the annealing operation [6,7]. Therefore, to the best of our knowledge, we firstly proposed to introduce an Ta_2O_5 insulator between the ferroelectric thin film and the Si. In this work, we have investigated the electrical properties of $Pt/SBT/Ta_2O_5/Si$ for the Metal/Ferroelectric/Insulator/Semiconductor (MEFIS) field effect transistor.

2. Experimental

Ta_2O_5 films were deposited on p-type (100) Si substrates by rf-sputtering of Ta_2O_5 target (purity=99.99%) in the reactive oxygen ambient. $Sr_{0.8}Bi_{2.4}Ta_2O_9$ films were prepared by metal organic decomposition (MOD) method on Ta_2O_5/Si substrate and baked subsequently at 250°C and 400°C for 5 min. These processes were repeated for the multi-layered structure. The SBT films were post annealed at 800°C for 1hr in the oxygen ambient. A top Pt electrode of 2×10^4 μm^2 diameter was patterned for the MEFIS capacitor and the capacitors were annealed again at 800°C for 30 min. The crystallinity of $SBT/Ta_2O_5/Si$ structures with different O_2/Ar gas flow ratio in Ta_2O_5 deposition was characterized by X-ray diffraction (XRD) measurement. The electrical properties were characterized by C-V and I-V measurement using HP 4284A and 4140B. The composition of SBT films were analyzed by wavelength disperse spectrometry (WDS). The depth profile of $SBT/Ta_2O_5/Si$ structure was analyzed by auger electron spectroscopy (AES).

3. Results and Discussion

Figure 1 shows the XRD patterns of $SBT/Ta_2O_5/Si$ after annealing at 800°C for 1hr. The phases of Ta_2O_5 and Ta metal are shown as the SBT films are deposited on Ta_2O_5/Si grown in ambient without O_2. These phases induce the charge injection and the degradation of electrical properties.

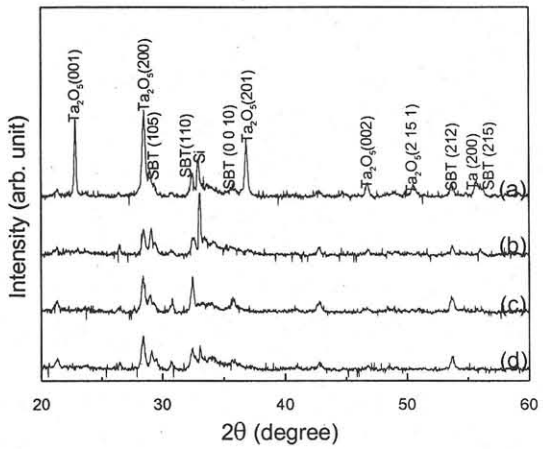

Fig. 1 XRD patterns of $SBT/Ta_2O_5/Si$ thin film after post annealing at 800℃; (a) 0 %, (b) 20 %, (c) 40 %, and (d) 60 % O_2 gas flow ratio of Ta_2O_5 sputtering condition.

Figure 2 shows the C-V characteristic of the $Pt/SBT/Ta_2O_5/Si$ structures with the different O_2/Ar gas flow ratios. The memory window of the MEFIS structure has maximum value under the flow ratio of 20 %. However, in the case of Ar ambient without O_2, typical C-V curve of MEFIS structure is not shown due to the charge injection.

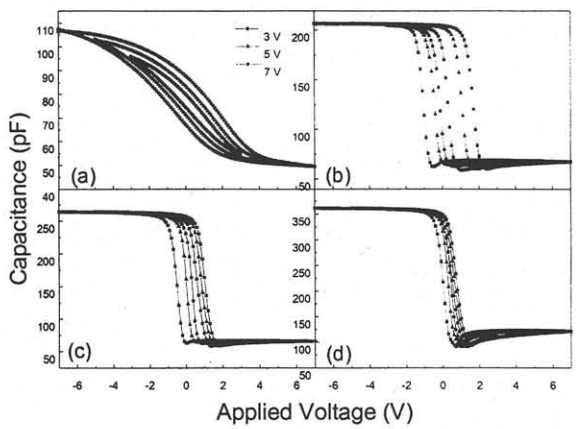

Fig. 2 C-V characteristics of $Pt/SBT(195nm)/Ta_2O_5/Si$ structure ; (a) 0 % , (b) 20 %, (c) 40 % , and (d) 60 % O_2 gas flow ratio of Ta_2O_5 sputtering condition.

Figure 3 shows the current-voltage characteristics of MEFIS structures. The leakage current in MEFIS structure at 20 % O_2 gas flow ratio is lower than that deposited in only Ar flow. It indicates the increasing of leakage current due to the Ta metal phase. These results indicate that the 20 % O_2 gas flow ratio is the optimum deposition condition of Ta_2O_5 layer with good electrical characteristics of MEFIS structures.

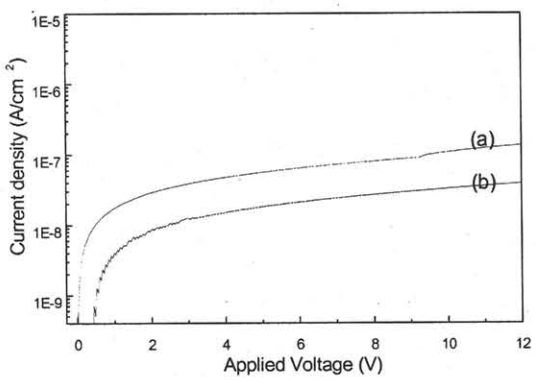

Fig. 3 I-V curves of Pt/SBT(195nm)/Ta_2O_5(36nm)/Si structure; (a) 0 %, and (b) 20 % O_2 gas flow ratio of Ta_2O_5 sputtering condition.

Figure 4 shows the C-V characteristics of MEFIS structures with the different thickness of 27 nm, 36 nm, and 54 nm thick Ta_2O_5 films, respectively. In Ta_2O_5 layer thickness of 36 nm, the memory window has the maximum value of 0.5~2.8 V at applied voltage of 3~7 V. It is thought that the memory window of MEFIS structure increases with decreasing Ta_2O_5 layer thickness. However, the MEFIS structure with 27 nm thickness of Ta_2O_5 layer has the lower memory window. Therefore, it is founded that an optimum thickness exists because an insulator with a very thin thickness cannot prevent reaction between the ferroelectric and Si. We have the maximum memory window in MEFIS structure with Ta_2O_5 layer thickness of 36 nm

The auger electron spectrometry (AES) depth profile of SBT/Ta_2O_5(36 nm)/Si structure is shown in Fig. 5. As shown in Fig. 5, there is no inter-diffusion between SBT and Si.

4. Conclusions

The Ta_2O_5 layer was firstly proposed as insulator layer for MEFIS structure. The optimum condition for memory window of MEFIS structure was investigated with the variation of Ar/O_2 gas flow ratio for Ta_2O_5 layer deposition and the thickness ratios of the SBT/Ta_2O_5. At the 20 % O_2 gas flow ratio and the thickness of SBT(195nm)/ Ta_2O_5(36nm), the maximum memory window in MEFIS was 0.5 - 2.7V in the applied voltage range of 3 - 7V. These memory windows will satisfy the practical application of the NDRO-FRAM operating at low voltage.

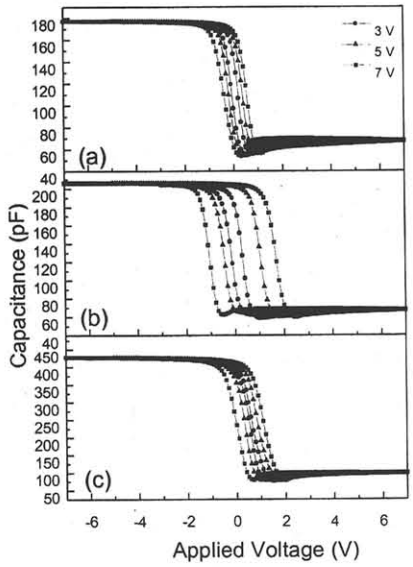

Fig. 4. C-V characteristics of (a) Pt/SBT(195nm)/Ta_2O_5/Si structure with the different thickness of (a) 27 nm, (b) 36 nm, and (c) 54 nm Ta_2O_5 film.

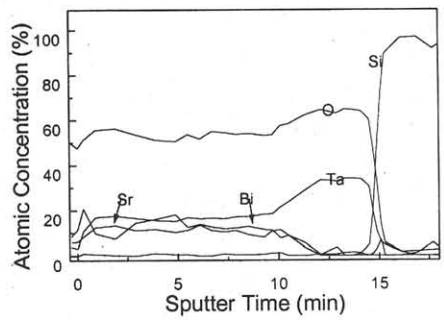

Fig. 5. AES depth profile of SBT(195nm)/Ta_2O_5(36nm)/Si thin film after post annealing at 800℃.

References

[1] J. F. Scott and C. A. Paz de Araujo, Science, **246**, 1400 (1989).

[2] K. Sugibuchi, Y. Kurogi and N. Endo, J. Appl. Phys., **46**, 2877 (1975).

[3] C. A. Araujo and G. W. Taylor, Ferroelectrics, **116**, 215 (1991).

[4] E. Tokumitsu, K. Itani, B. K. Moon and H. Ishiwara, Jpn. J. Appl. Phys. **34**, 5202 (1995).

[5] Y. Tarui, IEEE Int. Electron Devices Meet (1994).

[6] T. S. Kalkur, J. Kulkami, Y. C. Lu, M. Rowe, W. Han and L. Kammerdiner, Ferroelectrics, **116**, 135 (1991).

[7] T. S. Kalkur, B. Jacobs and G. Argos, Integr. Ferroelec. **5**, 177 (1994).