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A Novel P-Channel Flash EEPROM Cell with Simple Process and Low Power Consumption

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I. Introduction

The coming system on a chip (SOC) era strongly needs embedded technology. Flash EEPROM has widely been accepted as the memory of choice for program and data storage. Embedded flash EEPROM can offer enhanced system performance and added many advantages [1]. Low overall production cost of the logic products with integrated flash EEPROM is often the primary concern for embedded applications. For this reason, a robust flash EEPROM cell that is compatible with the existing host logic process without added tight process controls is a key criterion for use in embedded applications.

In this paper, for the first time, we demonstrate the feasibility of the **Simple p-channel flash EEPROM cell** [2], which requires only a reduced number of processing steps. It uses FN tunneling mechanism for programming and erasure operations, and provides a solution for disturb free operation and low power consumption.

II. Process Features

The flash memory employs twin well, double layers of polysilicon and three layers of metal based on 0.35μm CMOS process, and has the feasibility of shrinkage down to 0.25μm technology. Memory cell itself requires two additional masks, one for defining floating gate region and the other for defining thick gate oxide region for HV devices. The effective thickness of tunnel oxide and ONO is 85Å and 240Å, respectively. The key process parameters are described in Table I. Fig. 1 shows the top view, cross-section view, and TEM picture of memory cell along the bit-line direction.

III. Cell Structure

The gate length and width of the memory cell is 0.35μm and 0.5μm, respectively. Based on this configuration, high gate coupling ratio (GCR) of 74% can be achieved. The schematic fabrication process flow is demonstrated in Fig. 2. First, a stacked layer of the tunnel oxide and the floating gate (FG) polysilicon is formed. After the patterning of FG, interpoly dielectric layer (ONO) and the control-gate (CG) polysilicon are deposited. Next, the CG is defined by patterning these two layers, following that, p+ S/D implantation is carried out.

IV. Cell Characteristics

Table II summarizes the bias conditions during program, erasure, and read operations. Programming of the cell is achieved with 14V on the CG, 0V on the drain and N-well, and source floated. While erasure is done with 16V on the drain and N-well, 0V on the CG, and source floated. Typical programming and erasure characteristics are shown in Fig. 3 and 4. Accomplishment of programming and erasure operation is designated as cell threshold voltage higher than −1V and lower than −4.5V, respectively. Both of the programming and erasure time is less than 5msec under nominal bias voltages. Since only FN tunneling mechanism involves during programming and erasure operations on the selected cells, the requirement of low power consumption can be fulfilled. Note also that the self-limiting program characteristics can be achieved by the 3-transistor feature of Simple p-channel flash EEPROM cell, which prevents the memory cells from the issue of over-program.

Read of the cell is achieved with −2.5V on the CG, and −1V on the drain. I_D-V_G and I_D-V_D characteristics of the cell are shown in Fig. 5 and Fig. 6. To check the immunity of disturbance during erasure operation, the programmed and erased cells were stressed with 17V on the N-well, 0V on the CG, 5V on the drain, and source floated. No disturbance effect can be observed up to 1ksec stress time, as shown in Fig. 7. Fig. 8 illustrates the cycling result of a single cell at room temperature. Good endurance up to 1M cycles is achieved in terms of small window closure. Fig. 9 shows the cycling evolution on drain leakage current. Drain leakage current increases with cycling number. The degradation might be due to the holes, which can be accelerated by the lateral electric field during erasure operation. The holes gain enough energy, are injected into the tunnel oxide and cause damages [3].

V. Conclusion

A highly manufacturable **Simple p-channel flash EEPROM cell** has been demonstrated. Low power consumption, disturb free, and good endurance performance have also been achieved.

Acknowledgement

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References

[1]. J. C. Kuo *et al.*, *Int'l NVM Tech. Conf.* 1998, p.28.
[2]. J. M. Caywood *et al.*, *NVSMW* 2000, p.119.
[3]. J. Chen *et al.*, *IEDM Tech. Dig.* 1995, p.331.

Table I. *Key Process Parameters*

	Process Parameters
Tunnel oxide	85 Å
ONO (effective)	240 Å
Field oxide (LOCOS)	5000 Å
FG polysilicon	2000 Å
CG polysilicon	2500 Å

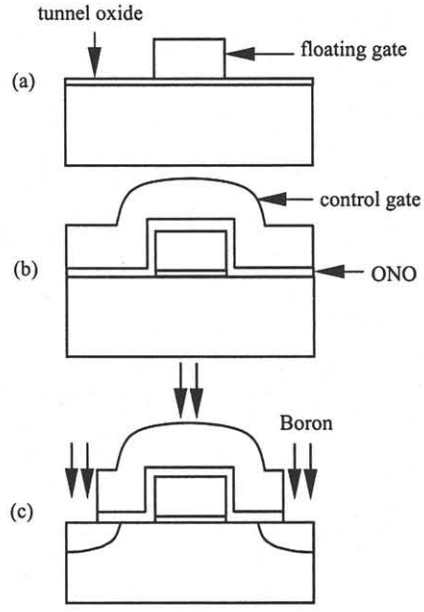

Fig. 2. Schematic process flow of the memory cell. (a) tunnel oxide formation, and floating gate polysilicon deposition, implantation, annealing and patterning, (b) ONO(thermal-oxide/nitride/HTO) formation, and control gate deposition, (c) control gate patterning, and p+ S/D implantation.

Table II. *Typical Bias Conditions*

	V_D	V_{CG}	V_S	V_{NW}
Program	0	14	Float	0
Erase	16	0	Float	16
Read	1.5	0	2.5	2.5

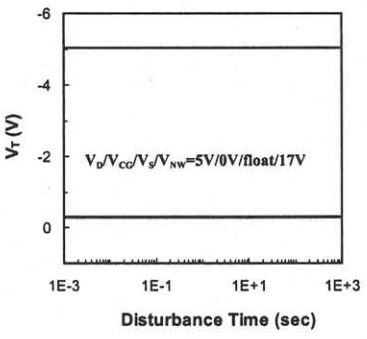

Fig.7. Disturbance characteristics of the programmed and erased cell.

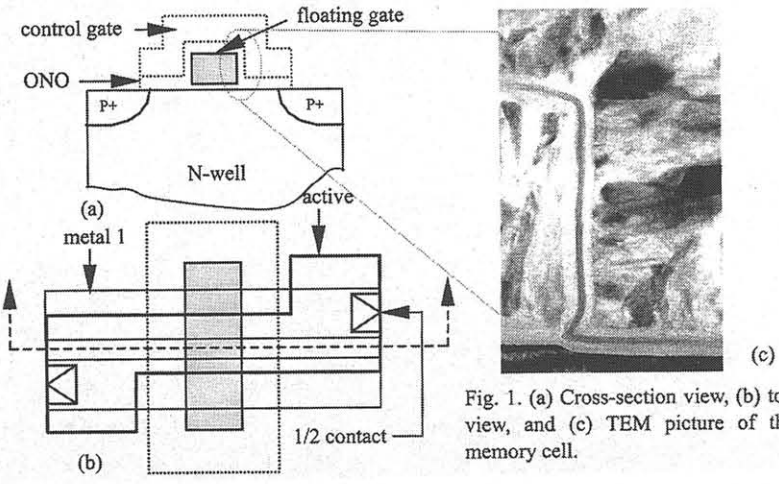

Fig. 1. (a) Cross-section view, (b) top view, and (c) TEM picture of the memory cell.

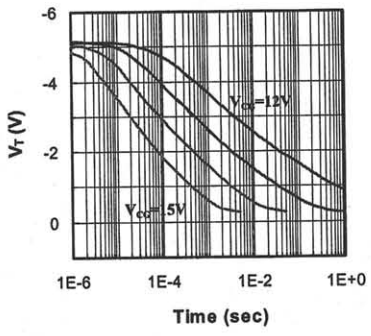

Fig.3. Programming characteristics of the cell. V_D=0V, V_{CG}=12-15V, V_S=floated, V_{NW}=0V.

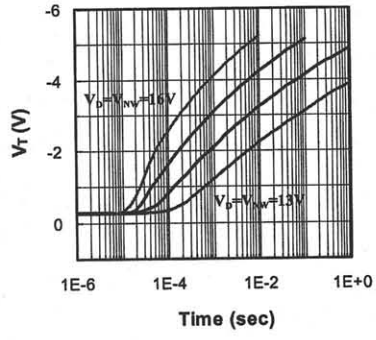

Fig.4. Erasure characteristics of the cell. V_D=V_{NW} =13-16V, V_{CG}=0V, V_S=floated.

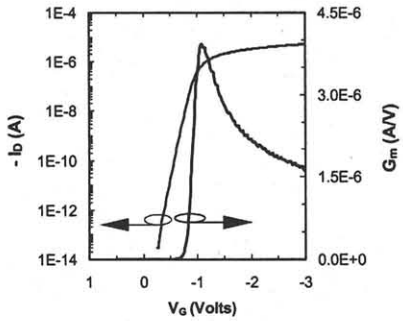

Fig.5. I_D-V_G characteristic of a programmed cell. V_D=-0.1V, V_S=V_{NW}=0V.

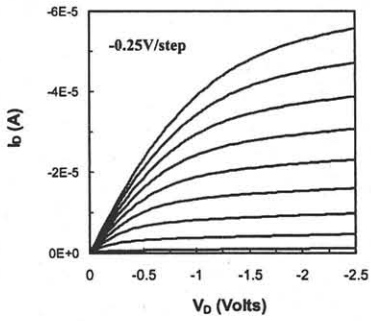

Fig.6. I_D-V_D characteristic of a programmed cell. V_G=-0.5V to -3V, V_S=V_{NW}=0V.

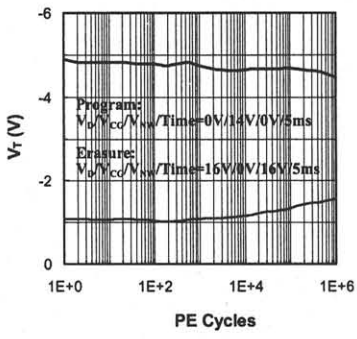

Fig.8. Cycling result of a single cell.

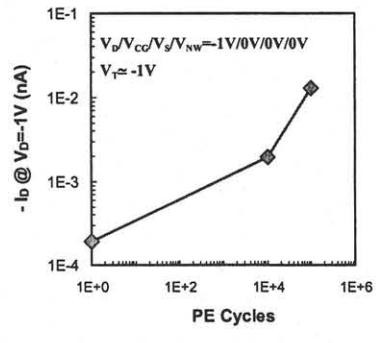

Fig.9. Leakage current evolution of the programmed cell vs. PE cycles.