Electrical Characterization of a Triple Self-Aligned Split-Gate Flash Cell for 0.18 \mu m Embedded Application


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Abstract

Electrical parameters were studied for the 0.18\mu m triple self-aligned (SA3) split-gate Flash cell which has successfully been embedded in a high performance CMOS logic process with copper interconnects [1]. A novel SA3 process integration together with high temperature oxide (HTO) process provide a compact cell and high degree of modularity with excellent high voltage (HV) characterization. The new Flash cells are suitable for low voltage applications due to programming by Source-side injection (SSI) and erasing by poly-poly tunneling.

Introduction

The advantages of the split-gate flash memory cells are the efficient programming [2], no over-erase [3], and low power consumption. With 2T per unit cell, compact split-gate layouts and processes competitive with NOR in size and performance, are a challenge. Recently, a novel triple self-aligned (SA3) split gate flash memory cell has been successfully embedded in a 0.18\mu m high performance CMOS logic process [1]. In this paper, the electrical characteristics and performance of the SA3 split-gate flash cell will be presented along with the discussions for the cell structure, the operation condition, and the integration process.

Process Integration

The key point of the SA3 cell structure is to use only one mask to form the floating gate (FG), the source contact, and the control gate which acts as the wordline (WL). The triple self-aligned attributes are: 1) the FG is self-aligned to the active region (RX) defined by the intersection of FG and RX, 2) the source contact, shared between two adjacent mirrored cells is self-aligned to FG, and 3) the WL is self-aligned to FG. Thus, a single FG mask defines the entire memory cell, eliminating alignment issues. Fig. 1 shows the schematic cross section of the 2T SA3 flash cell.

The SA3 flash cells were embedded in a standard high performance CMOS logic process flow with some new and modified features. The composite of the pad films is to add the FG polysilicon layer between the pad oxide and the pad nitride for the shallow trench isolation (STI). The pad oxide also serves as the FG tunnel oxide. After the STI formation, the FG mask is used to define the FG polysilicon trench. The tips at the corners of the FG polysilicon are created by natural curvature of the selective RIE stop. The final length of FG is determined by the TEOS spacer which also aligns the source contact area and the WL with FG. The length of the control gate is determined by the WL polysilicon thickness. Another key process feature in this study is the introduction of the high temperature oxidation (HTO). The composite oxide formed by the HTO plus the rapid thermal oxidation (RTO) is the dielectric material between the WL polysilicon and the substrate, and between the WL polysilicon and the FG polysilicon around the tip. A standard resist etch back process is used to form the HV/LV dual gate oxides. After the deposition of WL polysilicon, the standard high performance CMOS logic processes are followed to complete the integration.

Device Characteristics

Fig. 2 shows the charge-to-breakdown (Qbd) results for HTO composite oxide and thermal oxide. The results indicate that the reliabilities for the HTO oxide and the thermal oxide are similar. This is also supported by the comparison of the breakdown voltage distributions for both oxides as shown in Fig. 3. The breakdown voltage of ~21V for HTO composite oxide is two times higher than the maximum operation voltage. Fig. 4 indicates the low leakage of the HTO oxide. The HTO tunneling oxide thickness is 16.5nm which has been confirmed by both in-line and bench C-V measurements. The interface state density for the HTO oxide was calculated as 3.6E10 (cm2) from the charge pumping measurement as shown in Fig. 5. Fig. 6 shows the HV device characteristics for n-channel.

The electrical characteristics for the SA3 Flash cells which could be found in another paper [1] indicate the high CHE programming and poly-to-poly erasing efficiency. Fig. 7 shows the typical programming and erasing times for a 2V threshold voltage window. The programming time is about 30\mu s with 9.5V at Source while 1.8V for WordLine. The erasing time for 2V Vt window is about 200ms with 11.5V to the WordLine while zero voltage for Source and BitLine. The programming currents and efficiencies data for the different Source bias shows that electron injection efficiency is 10 times better than the Drain side CHE injection. With less than 2\mu A/cell, extensive parallel programming operation could be applied.

Conclusion

A new triple self-aligned (SA3) split-gate flash cell has been demonstrated for 0.18\mu m embedded application with superior electrical properties. The use of self-aligned structures allows higher density and compact cell layout without pushing lithographic limits or adding masking layers. HTO composite oxide provides an excellent dielectric layer underneath the Wordline poly. Source-side CHE programming and enhanced electric field tunneling erase allow highly efficient low power operations. A 4Mbit standard module is under evaluation.

References

Fig. 1 Schematic cross section of 2T SA3 cell.

Fig. 2 Charge to breakdown (Qbd) under constant current stress for both HTO and thermal oxides.

Fig. 3 Breakdown voltages for both HTO composite and thermal oxides.

Fig. 4 Leakage characteristics for both HTO composite and thermal oxides.

Fig. 5 Threshold voltages versus channel length for n-channel devices.

Fig. 6 Charge pumping current for HTO composite oxide.

Fig. 7 Programming and erasing times for a 2V threshold voltage window.