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A New Dual Floating Gate Flash Cell for Multilevel Operation

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1. Introduction

Multilevel Flash E^2PROM cells have been proposed to increase density of bits per unit area [1] in recent years. Most of the programming methods are either channel hot electrons (CHE) or Fower-Nordheim (FN) tunneling at the source/drain junction. To control the charge stored in the floating gate for multilevel operation, variable voltages or pulses are applied to the control gate or the drain/source junctions. The peripheral circuits become more complicated. Another category is multi-storage Flash memory. In this technology, the charges are stored in different locations of a Flash cell. The programming, erase and read conditions are similar to single-bit Flash cells, but the cell size is larger, such as the dual-bit split-gate (DSG) Flash cell [2]. Here, a new dual floating gate (DFG) Flash cell similar to Ref. [3] is proposed and illustrated in Fig. 1. Due to the different source and drain doping concentrations and doping energy is chosen, so it is not required to generate different voltages to achieve 4-level operation.

2. Operation Scheme

The geometry and dimensions of Flash cell are given in Fig. 1, in which the arsenic dosages/doping energies of J-1 and J-2 are $7.0\times10^{15}cm^{-2}$/30keVand $2.0\times10^{14}cm^{-2}$/40keV, respectively. With the similar junction depths using different doping energies, the doping concentration of J-1 is higher than that of J-2, which results in different amount of charge stored in the two floating gates during programming. The widths of the two floating gates (FG's) are 0.235μm. The gate coupling ratio is about 0.55. Table 1 lists the programming conditions for the four levels as well as erase and read operation. It is worth noting that the bias voltages are unchanged for any level programming, except switching to different electrodes. The channel hot electrons (CHE) and drain avalanche hot electrons (DAHE) injected into FG-1 or FG-2 depend on whether the applied voltage of J-1 (V_{J1}) is high or that of J-2 (V_{J2}) is high. To create "00" state, Level "01" programming condition is performed after Level "10" condition. In order to have wider level separation, the body contact (V_B) is floating to activate parasitic bipolar assisted programming [4].

Fig. 2 plots $|I_g|$ as functions of floating gate potentials (V_F) [4] for heavily and lightly doping junctions to explain the self-convergent technique. The reason is V_F decreases when the charges in the FG increase to certain value, for example, for single floating gate (SFG) structures programming to Level "00" with V_B=0, V_F may move from b to b' first using "10" bias condition. Then, the bias condition for Level "01" is applied and V_F may move from a" to a'. The total charge of Level "00" is even slightly less than that of Level "01", since V_B is grounded. However, for DFG cells, even though V_F of FG-2 has moved from b to b' using "10" bias condition, V_F of FG-1 is still close to Point a, which can be moved to Point a' using "01" bias condition. Therefore, Level "00" can be created using the 2-step method listed in Table 1.

To remove the charge in the FG's, channel Fowler-Nordheim (FN) tunneling was applied. It is not only more efficient than source/drain FN tunneling erase, but also more appropriate for erasing multilevel Flash cells with convergence [5].

3. Results

To illustrate the superior properties of the DFG structure, the SFG Flash cell are also shown in Figs. 3 and 4. The process parameters of both cells were the same, except FG-1 and FG-2 merged into one floating gate for the SFG structure. Figs. 3(a) and (b) plot the simulated V_{th}'s as functions of time for DFG and SGF cells, respectively. In Fig. 3(b), V_{th} variation is much smaller and unable to distinguish Levels "00" and "01" for SFG cells. Figs. 4(a) and 4(b) show the current through J-1 versus V_{cg} with V_{J1}=1V and V_{J2}=0 for the DFG and the SFG cells, respectively. The four levels can be identified clearly for the DFG cell, while only two levels can be observed in Fig. 5(b). Since the injection efficiency is not good enough for Level "10" of SFG cells, Levels "11" and "10" can not be identified clearly. Fig. 5 demonstrates V_{th} converging to the same values using channel FN tunneling mechanism.

4. Conclusions

In summary, the new DFG structure with simple bias conditions can generate four levels per cell with self-convergence using constant bias voltages. In addition, the charges in the two FG's can be removed completely using simple channel FN tunneling erase procedure with convergent characteristics. It should be a very good candidate for multilevel Flash memory applications in the future.

References

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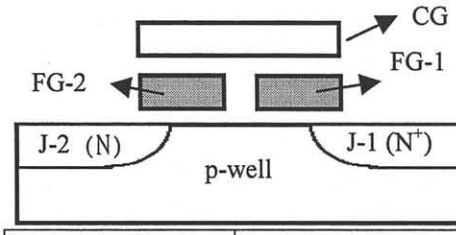
[3] M. Lorenzini, M.V. Rudan, G. Baccarani, *IEEE Trans. Components, Packaging, and Manufacturing Technology*, Part A, vol. 20, p. 182 (1997)
[4] M.-H Chi and A. Bergemont, *IDEM Tech. Dig.*, (1995) p. 271.
[5] Ph. Candelier, *et al.*, *IEEE International Reliability Physics Symposium*, (1997) p. 104.

[1] This work was done, while Shyh-Chyi Wong was with Winbond Electronic Corp., Hsinchu, Taiwan



Tunnel oxide	10 nm
ONO	Effective 20 nm
V_{TH} (Q=0)	1.5V
FG space	30 nm

Fig. 1 The geometry and dimensions of DFG Flash cell

Table 1 The bias conditions for program, erase and read

Program				
State	Bias conditions			
	V_{cg}	V_{J1}	V_{J2}	V_B
"11"	0V	0V	0V	0V
"10"	6V	0V	4V	0V
"01"	6V	4V	0V	0V
"00"	"10" (V_B=floating) + "01"(V_B=floating)			
Bias condition for erase				
V_{cg}	V_{J1}	V_{J2}	V_B	
0V	floating	floating	16V	
Bias condition for read				
V_{cg}	V_{J1}	V_{J2}	V_B	
3.8V	1V	0V	0V	

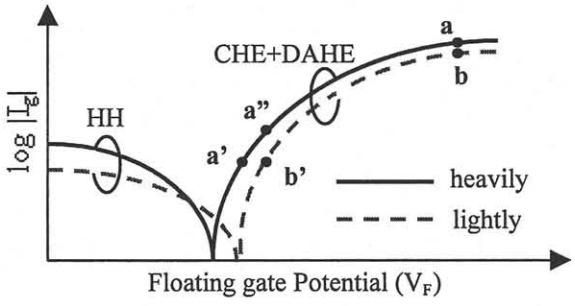


Fig. 2 General shape of gate injection current versus floating gate potential for different doping concentrations of junctions

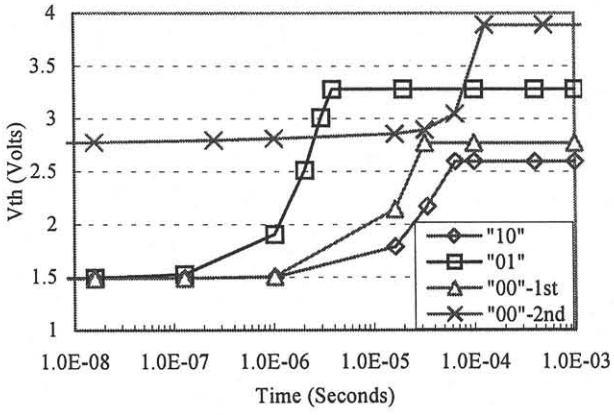


Fig. 3 (a) V_{th} can be distinguished pretty well for Level "00", "01" and "10" of the DFG cell. "00"-1st represents the first programming step, while "00"-2nd is the second step.

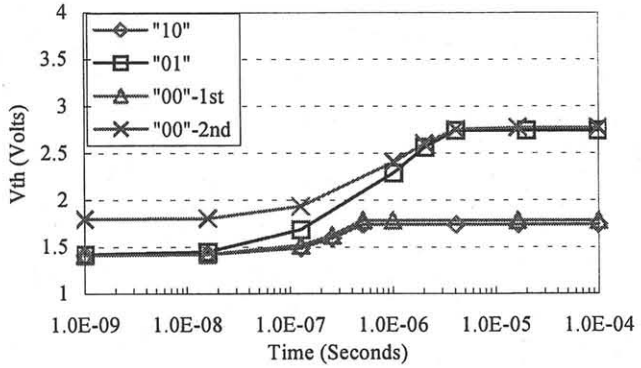


Fig. 3 (b) Separation of V_{th} for Level "00", "01" and "10" of the SFG cell is poor.

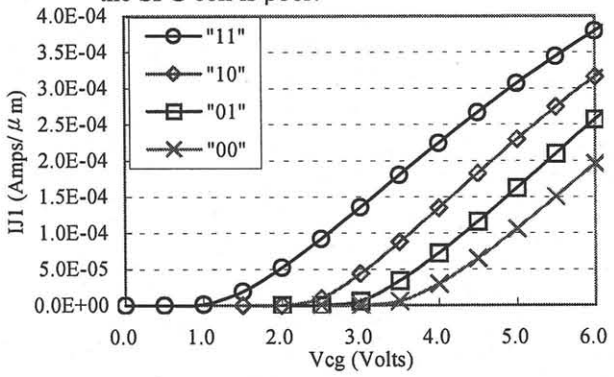


Fig. 4(a) Current through J-1 vs. control gate voltage (V_{cg}) is plotted for Level "00" to "11" of the DFG cell.

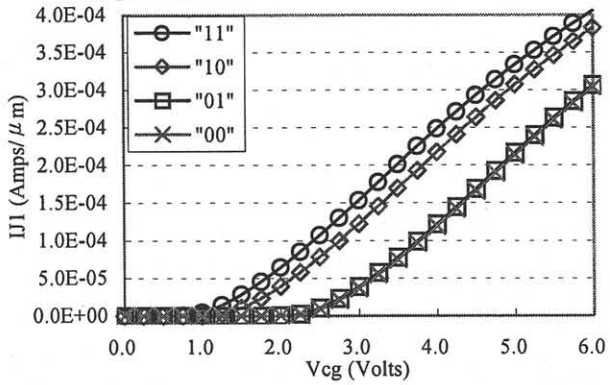


Fig. 4(b) Current through J1 vs. control gate voltage (V_{cg}) is plotted for Level "00" to "11" of the SFG cell.

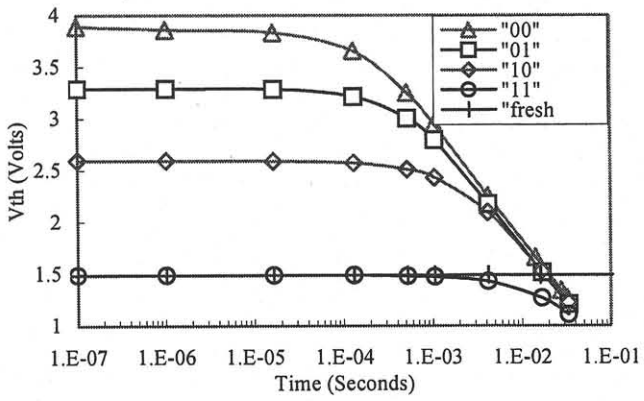


Fig. 5 V_{th} vs. time is plotted for Level "00" to "11" of the DFG cell during the erase procedures. V_{th}'s converge to the same value.