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A Body Effect Assisted NOR-Type (BeNOR) Multilevel Flash Memory

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1. Introduction

As the demand of flash memory density increases, advantages of device scaling and multilevel storage techniques become indispensable. As a result of the high operation voltage in NOR-type flash memory using Channel Hot Electron (CHE) programming, punchthrough becomes a major issue as the gate length scales [1]. Recently, J. D. Bude *et. al.* have proposed a low voltage programming scheme by applying negative back-gate bias to overcome this problem [2]. However, this art is not applicable for parallel multilevel storage of conventional NOR array architecture since its programmed states have nonlinear dependence on drain voltages.

In this work, we propose a novel Body Effect assisted NOR-type (BeNOR) flash memory with halo source to achieve low power programming and reliable multilevel storage. Multilevel storage, low power programming and high reliability are demonstrated in the novel BeNOR flash memory.

2. Experiment

The flash cell used in this study is the conventional ETOX structure with 10nm tunnel oxide and effective 17nm ONO layer as interpoly dielectric. The gate current of cells during programming in the following analysis is extracted from threshold voltage shift due to injected electrons.

3. Results and Discussion

Figure 1(a) illustrates the proposed cell structure and terminal voltage for BeNOR. The proposed timing diagrams for programming and erase operations of BeNOR are shown in Fig.1(b)(c). By varying bit-line voltage, programmed states can reach different levels in the period of T_{PGM} . Figure 2 demonstrates the programming characteristics of BeNOR with 2-bit storage. The programmed state exhibits almost linear dependence on bit-line voltage, which is hard to achieve in NOR-type flash with CHE or Channel Initiate Secondary Electron (CHISEL) programming. This linear dependence mainly comes from the shift of gate current spectra linearly governed by the gate to source overdrive, $V_{FG-BL}-V_{TH}$. Once the bit-line voltage difference dominates, the programmed states exhibit linearity dependence on bit-line voltage. The suggested multilevel programming conditions are listed in Table I. The period T_{ERS} indicated in Fig.1(c) for soft program ($T_{converge}$) for over-erase correction and tightening distribution of erased state, followed the channel FN ejection (T_{FN}) period.

Precise control of threshold voltages in flash memory is essential for achieving multilevel programming. The BeNOR programming shows better self-limited programming characteristic than CHE and Drain Avalanche Hot Electron (DAHE) injections as shown in Fig.3. BeNOR operation with a positive source voltage can sustain a higher drain voltage than those by CHE and DAHE due to the raise of the source bias. However, to achieve fast and precise programming, BeNOR cell needs further optimization for halo-implant in the source junction.

Figure 4 shows the convergence characteristics dependences

on bit-line voltage during programming operation. It is important to choose a suitable set of bit-line and word-line voltages for a desired programmed state under certain precision and speed criteria. Programming at a higher bit-line voltage results in slower convergence from different initial states and the more stable convergent state, as shown in Fig.4. The corresponding gate current spectra are depicted in Fig.5. The convergent characteristic is governed by the slope of I_G vs. $V_{FG-BL}-V_{TH}$. A small V_{BL} causes steeper slope at high V_{FG-BL} , therefore results in initial faster convergent speed. In addition, high V_{BL} leads to the more abrupt shoulder in the low V_{FG-BL} regime and causes more stable converged threshold voltage. This explains the quite different V_{BL} dependent convergent characteristics in Fig.4.

Figure 6 compares the power consumption during programming of BeNOR and CHE to achieve the same threshold voltage window of 3V in 10 μ s. The power consumption is reduced as bit-line voltage increases under a fixed source-line bias condition. The power consumption for BeNOR ($V_{SL}=6.5V$) at $V_{BL}=2.0V$ is more than 5 times lower than that for CHE ($V_{SL}=5.5V$). Therefore, high bit-line voltage operation is feasible for low power programming.

Figure 7 shows the schematics of BeNOR array. Unselected word-lines and bit-lines are biased at 0V and floating, respectively. During programming of cells "A", cells "B", "C" and "D" suffers bit-line, source-line, and word-line disturbance, respectively. The bit-line disturbance time and programming time of erased state ("00") are compared in Fig.8(a). More than 10⁴ disturbance cycles can be sustained for the various source-line voltages. The unique source-line disturbance due to non-zero common source-line voltage is demonstrated in Fig.8(b). No obvious window closing is observed within 1 second. On cell endurance, only slight degradation in the erased state is observed after 10k cycles as shown in Fig.9. This threshold voltage increase is related to interface state generation which leads to g_m degradation during channel FN erase as shown in Fig.10. However, the unchanged programmed states are believed to be results of both g_m and electron injection degradations.

4. Conclusion

This paper discloses a new Body effect assisted NOR-type (BeNOR) flash memory for low power and multilevel storage application. Body effect assisted self-convergent programming is comprehensively studied. Accurate programmed states control is achieved by the linear dependence of V_{TH} on bit-line voltage for multilevel storage application. In addition, low programming power consumption is also accomplished through the bit-line body effect.

Reference

- [1] K. Prall *et. al.*, IEEE Trans. Elec. Dev., p.34, 12, 1987
- [2] J. D. Bude *et. al.*, IEDM Tech. Dig., p.279, 1997

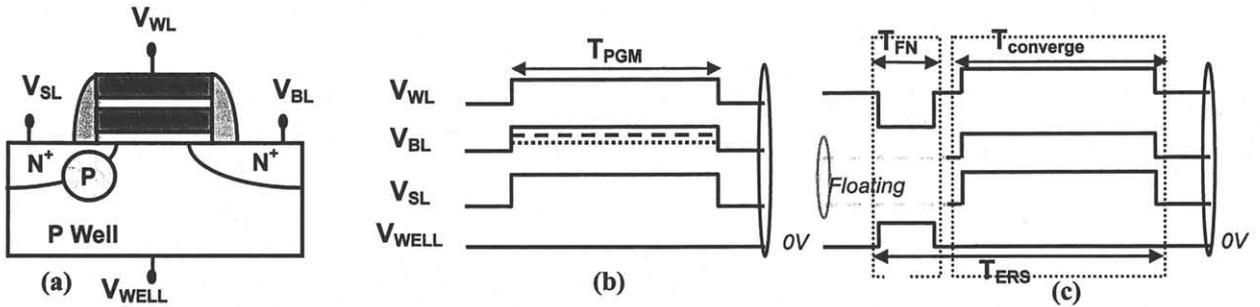


Fig. 1 (a) Proposed cell structure and terminals, (b) Timing diagram of multilevel program and (c) erase schemes for BeNOR.

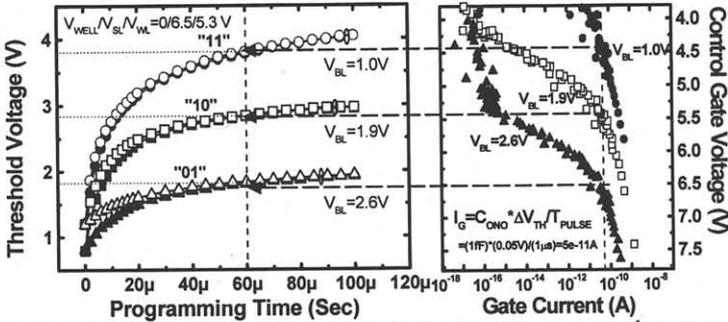


Fig. 2 Threshold voltage variations and gate current spectra under proposed BeNOR programming conditions for multilevel storage application.

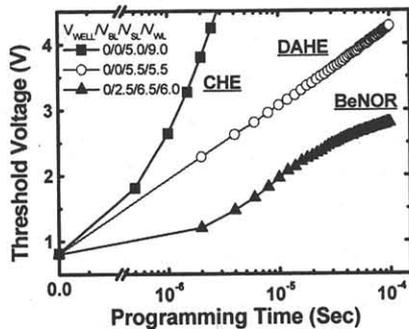


Fig. 3 Programming characteristics of BeNOR, CHE and DAHE.

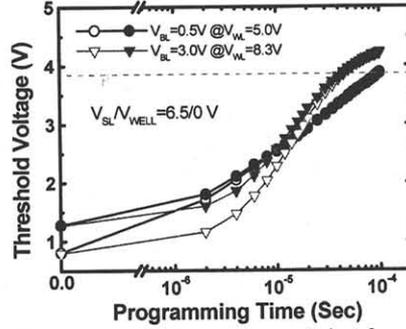


Fig. 4 Programming characteristics from the two initial states with various V_{BL} .

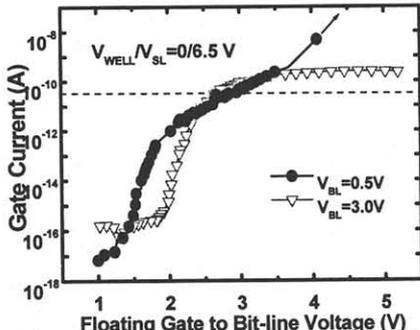


Fig. 5 Gate current spectra of BeNOR cell with various V_{BL} at $V_{SL}=6.5V$.

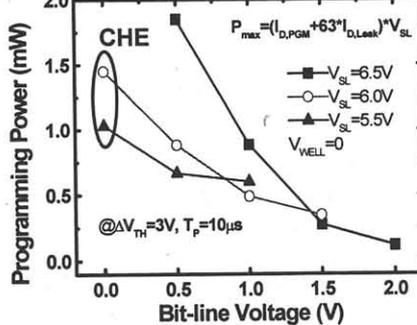


Fig. 6 Programming power for BeNOR with various V_{BL} .

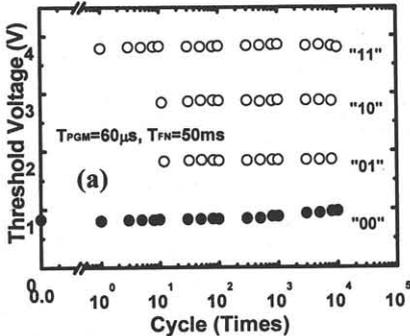


Fig. 9 Cell endurance with 2-bit storage

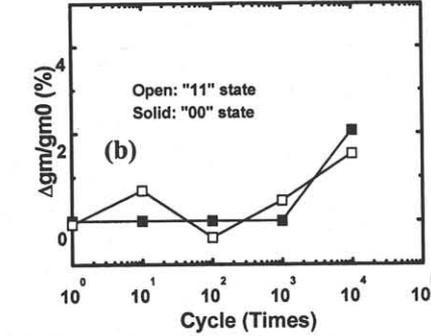


Fig. 10 g_m degradation during cycling.

Table I Suggested multilevel programming conditions.

Multilevel Programming of BeNOR				
	"11"	"10"	"01"	"00"
Selected V_{WL}	5.3V			
Unselected V_{WL}	0V			
Selected V_{BL}	1.0V	1.9V	2.6V	Floating
Unselected V_{BL}	Floating			
V_{WELL}	0V			
V_{SL}	6.5V			
T_{PGM}	60 μ sec			

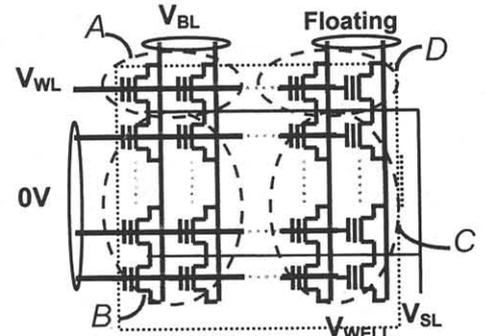


Fig. 7 Schematics of BeNOR array.

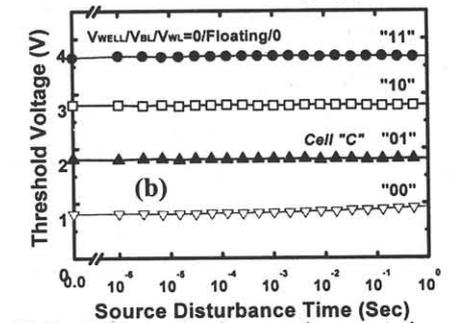
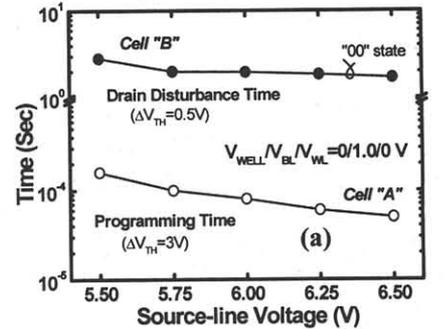


Fig. 8 (a) Drain disturbance and programming time vs. V_{SL} . Solid circle: $\Delta V_{TH}=0.5V$, open circle: $\Delta V_{TH}=3.0V$, (b) Threshold voltage variations as during source disturbance.