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On the Capacitance Coupling Ratios of a Source-Side Injection Flash Memory Cell[1]

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1. Introduction

The source-side-injection (SSI) Flash memory cell has been recently employed as the base of a multilevel storage technology [1]. With the source-follower read method and cumulative programming technique, precise amount of charge can be stored into and accurately sensed from the SSI cell [2]. In this paper, we report a new method for measuring the capacitance coupling ratios of non-volatile memory cells as applied to the SSI Flash cell. Conventional extraction methods [3, 4] are complicated by the presence of the select transistor. In this work the coupling ratios of a source-side injection Flash memory cell are extracted from source-follower voltage (Vsf) measurements of the Flash cell and a reference cell, in the read mode.

The SSI Flash cell consists of a select gate (SG) transistor and a floating gate (FG) transistor merged in a split-gate configuration [5]. As shown in Fig 1, there are three terminals: the common source (CS), the drain or bit-line (BL), and the select gate. The reference cell is essentially the same as the Flash cell with floating gate accessible as a terminal.

This split-gate cell can be cast into a two transistor (2-T) model as shown in Fig. 2, where the SG and FG transistors are in series and connected via the common node C which serves as the virtual source of FG transistor and also as the virtual drain of the SG transistor[2].

2. Theory and Method

In general the floating gate voltage of the Flash cell can be written in differential form as follows:

$$\Delta V_{fg} = \alpha_{sg}\Delta V_{sg} + \alpha_{cs}\Delta V_{cs} + \alpha_b \Delta V_b + \alpha_c \Delta V_c + \left(\frac{\Delta Q_{fg}}{C_T}\right) \quad (1),$$

where the α_{sg}, α_{cs}, α_b, and α_c are the floating gate FG, common source CS, substrate B and common node C voltage coefficients respectively. C_T is the total capacitance of the floating gate; ΔV_{fg}, ΔV_{sg}, ΔV_{cs}, ΔV_b, and ΔV_c the differential voltages respectively; and ΔQ_{fg} the differential FG stored charge[3]. These coefficients, α's can be interpreted as "capacitance ratios", such that

$$\alpha_{sg} = \frac{C_{sg}}{C_T},\ \alpha_{cs} = \frac{C_{cs}}{C_T},\ \alpha_b = \frac{C_b}{C_T},\ \alpha_c = \frac{C_c}{C_T} \text{ and} \quad (2),$$

where C_{fg}, C_{sg}, C_{cs}, C_b, and C_c as depicted in Fig 1, representing the capacitances from floating gate FG to select gate SG, common source CS, to bulk (substrate) and to common node C respectively[4]. Assuming constant α's and C_T, Eq. (1) can be integrated, thus

$$V_{fg} = \alpha_{sg}V_{sg} + \alpha_{cs}V_{cs} + \alpha_b V_b + \alpha_c V_c + \left(\frac{Q_{fg}}{C_T}\right) + W_{fg0} \quad (3),$$

where W_{fg0} is an integration constant[5].

The capacitances in Eq. (2) are relatively independent of terminal voltages in the range of normal cell operation. Thus Eq. (3) should give a fairly good estimation of Vfg from the terminal voltages of a two transistor cell model[6], if the coupling ratios were accurately extracted using Eq. (1).

Two-Dimensional device simulations of the cell provide a means to confirm our assumption. Fig. 3 shows the simulated floating gate voltage Vfg of a cell with Qfg = 0 and bit-line current Ibl = 1uA at two select gate voltages, Vsg. Here the goodness of linear Vfg to Vcs relationship is demonstrated. No significant change in the slope, dVsf/dVcs, is observed as the cell is moving from low Vcs (1-2V, read) to high Vcs (6-12V, program). However the slope of high Vsg (= 4V, read) is consistently higher than that of low Vsg (= 2.3V, program), indicating the small effect of Vsg and Vcs inter-dependency, which is not accounted for in Eq. (3). Fig. 4 shows the simulated floating gate voltage Vfg of a cell with Qfg = 0 with Vcs, Vbl, and Vb grounded. A change of the slope dVsf/dVsg is clearly observable as the FG transistor gets turned on from subthreshold to inversion. Gate coupling is effectively enhanced as the depletion capacitor responds to the gate voltage [7]. Finally, Fig. 5 shows the simulated floating gate voltage of a cell with Qfg = 0 and bit-line current Ibl = 1uA, Vcs = 2V, the normal read condition. A nearly linear relationship of Vfg to Vsg is demonstrated.

3. Experimental Procedure and Results

The extraction of SSI cell coupling ratios is based on Eq. (1). The source follower voltage Vsf [2] is read at a constant bit line current Ibl=1uA. Basically the terminals, Vsg, Vcs and Vb are varied and the responses are measured in Vsf ($\cong$ Vc). The reference cell provides a direct estimate of floating gate voltage Vfg. Fig. 6 shows the Vsf to Vfg characteristics of a reference cell, which is used for the Vsf to Vfg conversion for the corresponding Flash cell. Table I shows a set of the four measurement conditions for a set of α's at the operating point of Vsg = 4.2V and Vcs = 2.2V. These measurements of Vfg, Vsg, Vcs, Vb and Vc (= Vsf) generate three linear equations in α's. With the fourth equation $\sum \alpha_i = 1$ and $\Delta Vc = \Delta Vsf$, a set of α's can be solved.

TABLE I Cell Biasing for Coupling Ratio Extraction

Description	Vsg	Vcs	Vb	Ibl
Operating point	4.2 V	2.2 V	0 V	1 uA
ΔVcs	4.2 V	2.0 V	0 V	1 uA
ΔVsg	4.0 V	2.2 V	0 V	1 uA
ΔVb	4.2 V	2.2 V	+0.2 V	1 uA

Table II shows the extracted coupling ratios for three cases. The results are fairly consistent even when the operating condition shifted and stored charge changed. Only αb shows a larger fluctuation due to its near zero value. Table III shows the effect of source follower read current Ibl (bit-line) on the extracted coupling ratios. Consistent results are obtained for three decades of Ibl. Table IV shows the extracted coupling ratios of reversed source follower read (in Fig. 2c). Consistent results are obtained for different cases. The αbl_r is near zero due to virtual drain. The αsg_r, SG coupling ratio of reverse read, is noticeably smaller than that of forward read, suggesting higher total cell capacitance C_T_r in this mode. Fig. 7 shows the subthreshold I-V of two cases of the same cell used in Table II, αsg_subth is 0.33, which is about 10~15% higher than that from Vsf method. Fig. 8 and Fig. 9 show the measured and modeled Vsf vs Vsg and vs. Vcs respectively. Poorer fit at low Vsg is related to SG transistor turn-off.

4. Conclusions

The Capacitance coupling ratios of a source-side injection Flash memory cell are extracted using a new method based on source-follower voltage measurement for a two-transistor cell model in the read condition. Validity of these coupling ratios and the two-transistor memory cell representation under programming condition are confirmed via two-dimensional device simulations. These parameters provide a solid base for a multilevel Flash cell model.

5. Acknowledgments

We would like to express our most sincere thanks to Winbond management for their support and encouragement.

[1] Work done formerly at Information Storage Devices Inc., a Winbond Company.
[2] This node "C" is well defined physically only when at least one of the two transistors is operating in the linear region. Otherwise it represents an artificial demarcation.
[3] Eq. (1) follows the standard definition of differential terminal charge [6], so we have:

$$\Delta Q_{fg} = \left(\frac{\partial Q_{fg}}{\partial V_{sg}}\right)\Delta V_{sg} + \left(\frac{\partial Q_{fg}}{\partial V_{fg}}\right)\Delta V_{fg} + \left(\frac{\partial Q_{fg}}{\partial V_{cs}}\right)\Delta V_{cs} + \left(\frac{\partial Q_{fg}}{\partial V_b}\right)\Delta V_b + \left(\frac{\partial Q_{fg}}{\partial V_c}\right)\Delta V_c$$

[4] Strictly speaking these α's are trans-conductances and $1 = \alpha_{sg} + \alpha_{cs} + \alpha_b + \alpha_c$ [6].
[5] Constant W_{fg0} includes the weighted flat-band voltages as seen by floating gate FG [7].
[6] This works particularly well if the cell is operating at a fixed small current. In our read the current is fixed, so the channel potential tracks closely to the virtual source voltage.

References

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[2] C.-M. Liu et al, *Extended Abstract of SSDM*, September, pp. 542, 1999.
[3] M. Wada, et al., *IEDM Digest of Technical Papers*, pp. 38, 1980.
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[7] M. Wong et al, *IEEE Electron Device Letters*, vol. 13, no. 11, pp. 566, 1992.

TABLE II Cell Coupling Ratios

Op point	Vsf (V)	α_{sg}	α_{cs}	α_b	α_c
A	0.709	0.299	0.507	0.001	0.192
B	0.709	0.295	0.514	0.002	0.189
A	1.036	0.295	0.517	0.004	0.184

Operating points:
A — Vsg=4.2V, Vcs=2.2V, Ibl=1uA, standard
B — Vsg=3.8V, Vcs=2.0V, Ibl=1uA

TABLE III Effect of Vsf Read Condition

Read Ibl	α_{sg}	α_{cs}	α_b	α_c
1uA	0.299	0.507	0.001	0.192
100nA	0.271	0.480	0.002	0.247
10nA	0.267	0.472	0.002	0.259
1nA	0.278	0.496	-0.001	0.228

Operating point: Vsg=4.2V, Vcs=2.2V

Read at 1uA: Vsf = 0.709V

TABLE IV Cell Coupling Ratios in Reverse Vsf read

Op point	Vsf (V)	α_{sg_r}	α_{bl_r}	α_{b_r}	α_{c_r}
A	0.709	0.230	0.004	-0.001	0.768
A	1.036	0.238	0.001	0.001	0.760
B	1.036	0.240	0.004	0.000	0.755

Operating points:
A — Vsg=4.2V, Vcs=2.2V, Ird=Ics=1uA,
B — Vsg=4.2V, Vcs=2.2V, Ird=Ics=1uA, but ΔVsg=0.1V, ΔVcs=0.1V
Vsf column refers to forward read at 1uA:

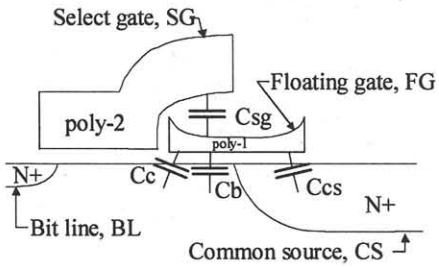

Fig 1 Diagram of split-gate cell capacitances. The floating gate capacitance is the sum of four components: Csg, Cc, Cb, and Ccs.

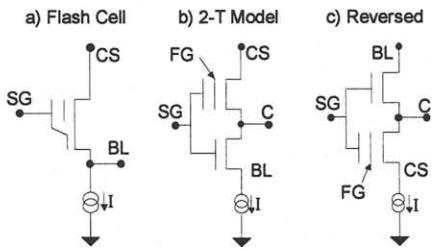

Fig 2 Circuit schematic symbols for: a) a flash cell during read, b) the two-transistor model. c) The reversed mode.

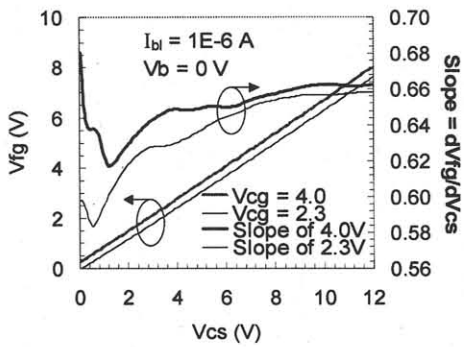

Fig. 3 Two-dimensional simulation results showing Vfg vs. Vcs, for two different Vcg conditions.

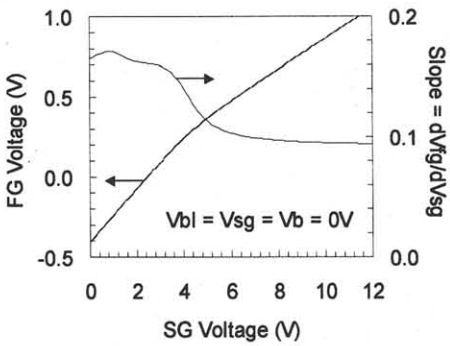

Fig. 4 Two-dimensional simulation results showing Vfg vs. Vsg, and the slope. Note how the slope changes when the channel is formed.

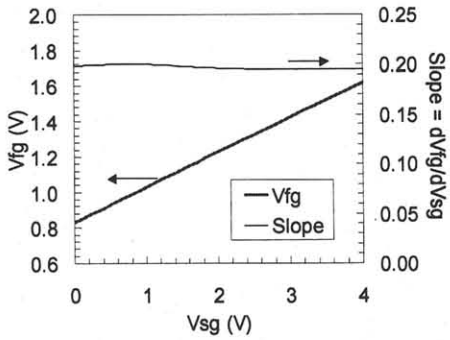

Fig. 5 Two-dimensional simulation results showing Vfg vs. Vsg, and the slope during read. Vcs = 2V, Ibl = 1uA.

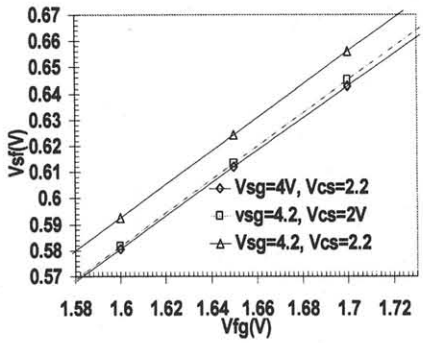

Fig. 6 This is Vsf vs. Vfg measured on a reference MOSFET. Six points are used to convert Vsf into Vfg for coupling ratio extraction.

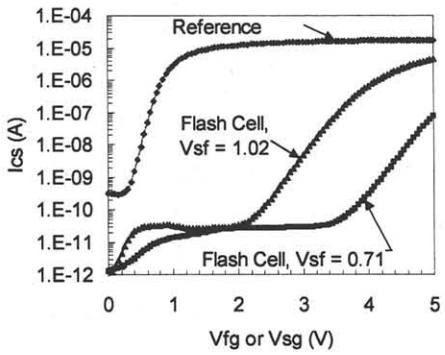

Fig. 7 Subthreshold I-V curves for a reference MOSFET and a flash cell, Vcs = 0.1V. The cell was measured with two different charge states.

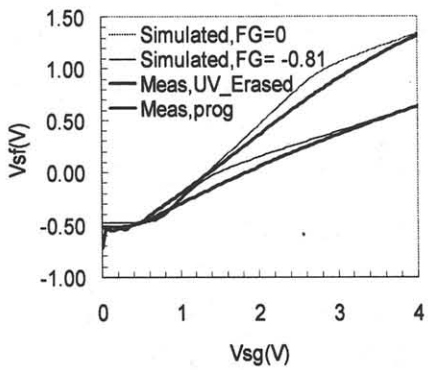

Fig. 8 Comparison of simulated and measured cell data showing Vsf vs. Vsg for two different charge states: UV Erased and programmed

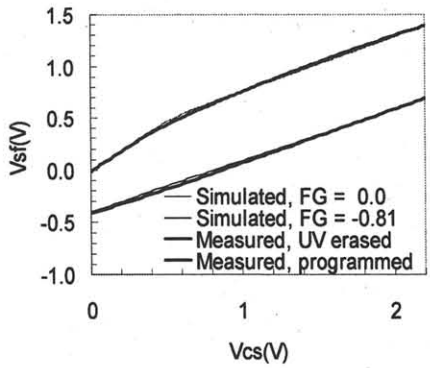

Fig. 9 Comparison of simulated and measured cell data showing Vsf vs. Vsg for two different charge states: UV Erased and programmed.