C-6-2

Analysis of Gate Disturb Degradation by Nitridation of Flash Tunnel Oxide

M. Arai, T. Hashidzume, T. Nitta, Y. Odake and I. Matsuo

ULSI Process Technology Development Center, Semiconductor Company, Matsushita Electronics Corporation

19, Nishikujo-Kasugacho, Minami-ku, Kyoto, 601-8413, Japan

Phone: +81-75-662-8906, Fax: +81-75-662-6196, e-mail: arai@krl.mec.mei.co.jp

Introduction

Nitrided tunnel oxide is one of the key technologies to improve the reliability in flash EEPROMs. Several authors have shown that nitrided tunnel oxide had higher charge to breakdown (Q_{BD}), reduced interface states and improved endurance characteristic compared with conventional tunnel oxide [1],[2]. However, the disadvantages of nitrided tunnel oxide have not been studied sufficiently. In this work, the enhancement of gate disturb with negative bias stress caused by increased hole trapping at the surface of tunnel oxide was found. Based on gate disturb characteristics, the desirable conditions of nitridation were discussed.

Experimental

Nitrided oxide films were formed on n-type and p-type substrates by processes shown in Table 1. Final thickness of each nitrided oxide was adjusted to about 8 nm. Q_{BD} and hole trapping was evaluated by constant current charge injection into tunnel oxide with accumulate mode in MOS capacitors. Flash memory cells were fabricated to evaluate gate disturb characteristics by a conventional stacked gate process. Gate disturb characteristics were measured by adjusting control gate voltage to have the same electric field at tunnel oxide after 1000 program/erase cycles.

Table 1 Nitridation parameters.

#Sample	SIO ₂ 8nm	SIO ₂ 7nm +N ₂ O 1nm	SIO ₂ 5nm +N ₂ O 3nm	SIO ₂ 8nm +NO 800°C	SIO ₂ 8nm +NO 950°C
Peak of Nitrogen Concentration [atmic%]		1.652	2.697	not measured	2.970
Base Oxide [nm]	8.01	6.81	4.86	8.01	8.01
Nitridation		N₂O 1050℃ 60s	N ₂ O 1050°C 205s	NO 800°C 60s	NO 950°C 60s
Total Thickness [nm]	8.01	8.15	7.98	8.03	8.11

Results and Discussion

A. Gate Disturb Characteristics

Fig. 1 shows gate disturb characteristics with negative bias stress. The threshold voltage shifts ΔV tm- increase as increasing thermal budget for N₂O-nitrided oxide. On the other hands, the degradation of ΔV tm- is not observed for NO-nitrided oxide. Fig.2 shows gate disturb characteristics with positive bias stress. The threshold voltage shifts ΔV tm+ are greatly reduced for both N₂O-nitrided oxide and NO-nitrided oxide. In the conditions of both SiO₂ 5nm+N₂O 3nm and SiO₂ 8nm+NO 950°C, almost the same improvement of ΔV tm+ can be achieved.

B. Hole Trapping into Nitrided Tunnel Oxide

Fig. 3 shows comparison of 50% cumulative failure of Q_{BD} between positive gate bias and negative gate bias. In positive bias, Q_{BD} increases with the increase of thermal budget for both N₂O-nitrided oxide and NO-nitrided oxide. However, in negative bias, Q_{BD} is degraded with the increase of thermal budget for both N₂O-nitrided oxide and NO-nitrided oxide. Similar gate polarity dependence is observed in gate voltage shifts by hole trapping during Fowler-Nordheim (F-N) stresses defined in Fig.4. In positive bias, hole trapping increases with the increase of thermal budget for both N₂O-nitrided oxide and NO-nitrided oxide and NO-nitrided oxide in CF-N) stresses defined in Fig.4. In positive bias, hole trapping increases with the increase of thermal budget for both N₂O-nitrided oxide and NO-nitrided oxide and NO-nitrided oxide.

suppressed in negative bias as shown in Fig. 5. It should be noted that little increase of hole trapping is achieved for NOnitrided oxide compared with N2O-nitrided oxide in positive bias. We now propose dual-quality-layer model, which can explain these results. In nitridation process, high quality layer is formed on the substrate side of tunnel oxide by nitrogen diffusion [3], but poor quality layer is concurrently formed on the region where nitrogen atoms do not exist as shown in Fig. 6. In positive bias, Q_{BD} increases because electrons pass through the high quality layer, but hole trapping increases because most holes are trapped at the poor quality layer. In negative bias, QBD is degraded because electrons pass through the poor quality layer, but hole trapping is suppressed because most holes are trapped at the high quality layer. One possible cause creating poor quality layer is diffusion of hydrogen atoms out of base oxide [4]. The little increase of hole trapping in positive bias for NO-nitrided oxide is explained by suppressed out-diffusion of hydrogen atoms due to the lower thermal budget.

C. Discussion

It is found that ΔV tm- depends on hole trapping at the surface of tunnel oxide as shown in Fig. 7. This result indicates that trapped holes at the surface of tunnel oxide enhance gate disturb with negative bias stress. On the other hands, gate disturb with positive bias stress is improved even if the trapped holes at the surface of tunnel oxide increase. This is due to the localized band modulation at the surface of tunnel oxide as shown in Fig. 8. In negative gate bias, electrons can easily tunnel through oxide because of the reduced barrier height at the surface of tunnel oxide. In positive gate bias, electron tunneling is not enhanced because the reduced barrier height at the surface of tunnel oxide never makes a contribution to enhancement of electron tunneling. Further, hole trapping at the bottom of tunnel oxide is suppressed by diffused nitrogen atoms, therefore, electron tunneling is extremely suppressed in positive gate bias as shown in Fig. 3. From these results, it is considered that ideal condition of nitridation should be lower thermal budget with higher nitrogen concentration. In conclusion, NO-nitridation at 950°C is the most applicable for flash tunnel oxide in this experiment because of the maximum suppression of gate disturb with positive bias and no degradation of gate disturb with negative bias.

Summary

The enhancement of gate disturb with negative bias stress caused by increased hole trapping at the surface of nitrided tunnel oxide was found. For NO-nitrided oxide, no degradation of gate disturb with negative bias stress and large improvement of gate disturb with positive bias stress were achieved because of its lower thermal budget with higher nitrogen concentration.

References

- 1) T. Arakawa et al., Jpn. J. Appl. Phys., 34, 1007 (1995).
- 2) M. Ushiyama et al., Ext. Abs. SSDM, 859 (1994).
- 3) Y. Okada et al., Appl. Phys. Lett., 61, 3163 (1992).
- 4) T. Hori et al., *IEEE Trans. Electron Devices*, ED-36, 340 (1989).



layer.



J=100[mA/cm²]

+Vg

SIO₂ 5nm +N₂O 3nm

J=100[mA/cm²]

+Vg

SIO2 8nm +NO 950°C

-2.2

ΔVtm-

-2.3 -2.4

High Quality Layer

Substrate

Substrate

293