# Simulation of Positive Oxide Trapped Charge Induced Leakage Current and Read-Disturb in Flash EEPROMs

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## Abstract

The mechanisms and transient behavior of hot hole stress induced leakage current (SILC) in tunnel oxides are investigated. A charge separation technique is used to characterize individual electron and hole components in SILC. A time-dependent positive trapped charge assisted tunneling model is developed. Related read-disturb characteristics in flash EEPROMs due to hot hole SILC are measured and simulated.

## Introduction

Hot hole stress during erase is generally believed to be the major cause of SILC and data retention degradation in flash EEPROMs. In this work, the role of positive oxide trapped charge in SILC and its significance to read-disturb in flash EEPROMs will be charcaterized and calculated.

Conventional gate n-MOSFET's with a long source edge were used to measure hot hole SILC directly. The devices have a gate length of  $0.7\mu$ m and a tunnel oxide thickness of 90Å. After edge FN stress or negative gate bias channel FN stress, we observe a *stress induced substrate current* as well as SILC (Fig.1). We will show by numerical simulation that the low-field substrate current (Ib) arises from positive oxide charge (+Qox) detrapping. In Fig. 2, we plot the stress induced Ib versus SILC at different stress times. A linear correlation between them is noticed, no matter by either channel FN stress or edge FN stress. This correlation provides evidence that the SILC is related to +Qox creation. BTBT hot hole injection and anode hot hole injection are the responsible mechanism for +Qox generation in the two stresses, respectively.

Various SILC components in a hot hole stressed oxide are illustrated in Fig. 3. Icat denotes positive oxide charge assisted electron tunneling current, Ih represents positive oxide charge detrapping current and Ie is negative oxide charge detrapping current. In the current stress conditions, Ie is negligible, as compared to Icat and Ih. At a positive measurement gate bias, Icat flows from the gate to the source and the drain while Ih flows to the substrate. By using a charge separation technique (Fig. 4), we can obtain the electron current component (Icat) and hole current component (Ih) separately.

## Hot Hole SILC Modeling

In our model, a Coulombic potential well (Eqs. (1) and (2) in Fig. 3) caused by a positive trapped charge is incorporated in the electron tunneling barrier. The transient effect of the electron and hole leakage currents Icat and Ih can be formulated by Eqs. (6) and (7). The parameters used in simulation are shown in Fig. 3. To our knowledge, *this is the first time to simulate the transient response of* +Qox

*induced leakage current* and corresponding read-disturb behavior.

The time-dependence of Ig and Ib at different measurement oxide fields are shown in Fig. 5. The symbols represent measurement data and the solid lines are from simulation. A careful study reveals that the hot hole SILC (mostly electron tunneling current Icat) and Ib (hole tunneling current) exhibit slightly different time-dependence, i.e.,  $Ib \propto t^{-1}$  and  $Ig \propto t^{-n}$  with n<1. The  $t^{-n}$  time-dependence of Ig was also reported by other groups (n=0.7) [1]. Fig. 6 shows the field dependence of the various leakage current components in an edge FN stressed device. The measured hole detrapping current (Ib) is nearly independent of oxide field, in agreement with the calculated result. In contrast, Ig exhibits a stronger field dependence. The reason is that the major part of the Ig is electron tunneling current, which has a smaller effective tunneling barrier.

## **Read-Disturb** Characteristics

The read-disturb characteristic due to the transient effect of the hot hole SILC is simulated. In Fig. 7, a threshold voltage change ( $\Delta Vt$ ) in a flash EEPROM due to the SILC transient is plotted. Note that from the tunneling front model  $\Delta Vt$  resulting from oxide charge trapping/detrapping should be linearly proportional to the logarithm of time [2]. Our simulated power-law dependence in Fig. 7 is attributed to the Icat component, which has a t<sup>-0.75</sup> dependence around Eox=5MV/cm. The slope in Fig. 7 is therefore about (1n)≈0.25. In Fig. 8, we measured the  $\Delta Vt$  versus read-disturb time in a stacked gate flash EEPROM device (tox=90Å) after 10<sup>5</sup> P/E cycles. Edge FN erase is used in the cycling stress. A power-law relationship is obtained with a power factor about 0.3. A similar measurement result with a power factor of 0.28 was reported by Kato et al for tox=85Å [3].

#### Conclusion

We conclude that +Qox creation plays an important role in SILC and related read-disturb characteristics in channel FN and edge FN erase conditions. A power-law dependence of  $\Delta$ Vt on read-disturb time, resulting from the transient effect of Icat, is derived from our numerical simulation. Stress induced low-field Ib can be used as a monitor of positive charge assisted tunneling current.

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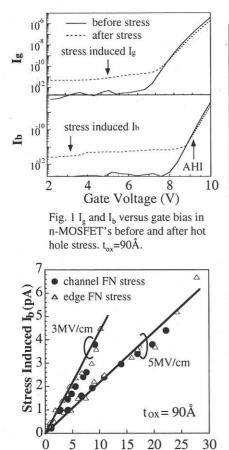


Fig. 2 Stress induced substrate current versus SILC measured at different stress times. The oxide field in measurement is 3MV/cm and 5MV/cm, respectively.

Stress Induced Ig (pA)

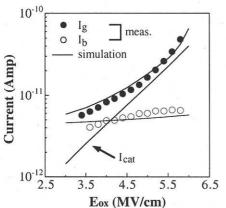


Fig. 6 Field dependence of electron tunneling current ( $I_{cal}$ ), substrate current ( $I_h$ ) and gate current ( $I_g=I_{cat}+I_h$ ). Negative oxide charge detrapping current is negligible. The symbols represent measurement data points at t=0.2sec and the lines are from simulation.

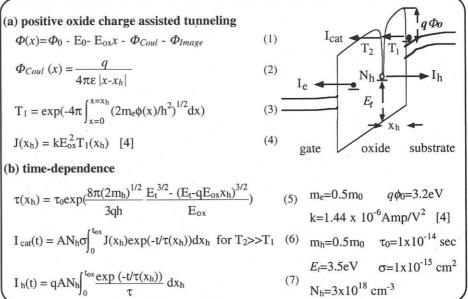
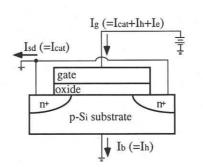


Fig. 3 Numerical simulation of SILC and substrate current in a n-MOSFET by hot hole stress.  $I_{cat}$  denotes positive oxide charge assisted tunneling current.  $I_h$  represents positive oxide detrapping current.  $T_1$  and  $T_2$  are the electron tunneling probability.  $E_0$  is the first quantization level in the inversion layer [4].  $\tau$  is the positive oxide charge tunneling time.  $N_h$  is the volumertic positive oxide charge concentration. A is the area of the stress region. Other variables have their usual definitions.



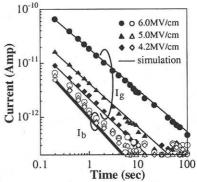


Fig. 4 Illustration of a charge seperation technique.

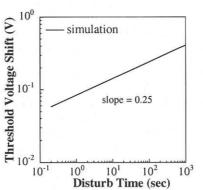


Fig. 7 Simulated threshold voltage shift versus read-disturb time in a flash EEPROM from the SILC in Fig. 5.  $E_{ox}$ =5MV/cm. A power law dependence is obtained with a power factor about 0.25.

Fig. 5 Simulated and measured  $I_g$  and  $I_b$  transients in a n-MOSFET by edge FN stress. The measurement field is 4.2MV/cm, 5.0MV/cm and 6MV/cm, respectively. The symbols represent measurement data points and the lines are from simulation.

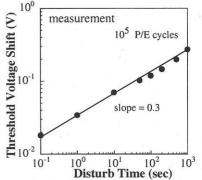


Fig. 8 Measured threshold voltage shift versus read-disturb time in a stacked gate flash EEPROM after 10<sup>5</sup> P/E cycles. Hot electron program and edge FN erase are used. The read-

disturb field is about 5MV/cm. The power factor is about 0.3.