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Screening for Flash Cells with Retention Related Defects

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1. ASTRACT

This paper presents a screening for Flash memories cells with retention defects related to charge loss. Other screenings already exist for this kind of rejects, but our study is aimed to an easier solution able to reduce testing costs.

2. INTRODUCTION

The production test flow of Flash Memories includes various steps of testing screenings combined with bakes with and without supply applied in order to detect all the possible functional, parametric and reliability-related defects. The Electrical Wafer Sort (EWS) aims to screen silicon related defects and to repair the dice. The Final Test (FT) checks the functionality of the device after assembly in stricter conditions with respect to the Data Sheet Specifications. The bakes performed between the testing phases help to screen retention related defects (charge loss/gain) of the cells, and of course cycling degradation of the array and the circuitry. This paper evaluates the screenings of the defects actually activated by the high temperature treatment of the devices as soon as possible, in order to reduce the cost due to the detection of a defective device in a further testing step.

3. EXPERIMENTAL

Our experience derives from testing of Flash cells in 0.35 um technology. We want to screen cells having defects causing charge loss. It is obtained performing a bake on the array fully programmed. In fact, the temperature is used as an accelerating factor for charges to move from the floating gate. We evaluated different samples of defects finding isolated cells losing charge for oxide defectivity, but also for other failing mechanism. Some cells have a slight different behavior: they lose charge when adjacent cells are erased, i.e. sharing charge with them. Two adjacent cells can share charge when they have very different charge content, i.e. one is erased and the other is programmed. Resistive paths between the floating gates cause this defective phenomenon. It is a mechanism similar to liquid sharing between two beakers connected by a pipe. If one beaker is full and the other is empty, a liquid flow through the pipe will be in place until the equilibrium is reached. In the same way, there can be a flow of charges between two cells if they have different charge contents, and a path exists between them. It is possible to detect cells with charge sharing defectivity programming up the array with a particular pattern named checkerboard (CK, zeros and ones alternatively located). This makes the cells one close to the other having very high differences in their charge content, determining a finite probability of charge sharing in case the floating gate of the cells is not properly isolated. A high temperature bake can then be used as accelerating factor for charge sharing. One can easily detect the dice with charge gain/loss related defects by verifying the content of the array at the next test. This approach anyway delays the detection of the defective parts and makes the testing flow complex and so heavy in terms of time, costs and resources for production purposes.

We want to find the possibility to remove the bake and the next screening, experiencing a single flow, but maintaining anyway the same testing coverage for all the above defects.

The threshold of a Flash cell is meant to be the minimum voltage applied to the gate in order to have 10uA of Drain-Source current Ids. Programming a Flash cell means cumulating charge in its floating gate, and implies its threshold to get higher. In an opposite way, erasing a cell results in removing charge from its floating gate and then getting a lower threshold. We define Vgmin as the higher value of a distribution of thresholds of an erased array, meaning that it is the minimum gate voltage that can be applied to all the cells of the array such that a minimum amount of Ids current can flow (read as a "1"). In the same way, Vgmax is the lower value of a distribution of threshold of a programmed array, meaning that it is the maximum gate voltage that can be applied to all the cells of the array such that still no current is flowing (read as a "0").

A screening can be implemented using the threshold measurements of the cells before and after programming. Starting from an erased array, programming a bit that could share charge with adjacent bits results in affecting their thresholds at least of a small delta. As a matter of fact such a screening has to check that during checkerboard programming, not programmed bits do not change their own threshold. The sequence then is: measure Vgmin of the erased distribution, that is the minimum control gate voltage to read whole array erased, logically All1; verify one and program CKN (Checkerboard Bar), that is program a bit every two, namely March Test but performed only on CKN; then read CK using Vgmin plus 200 mV as voltage value on the gates.

A correlation was performed on about 80000 dice tested first with a normal CK programming without any DeltaVgmin verification and after with the algorithm described before.

About 100 dice per wafer were failing with the new screening and were not detected by the previous. The failing dice showed bits with a threshold out of the distribution after the CK pattern programming, i.e. lower than the previously measured Vgmax.

We also measured the gain of failing and good cells to be sure that failing bits did not have structural differences that could affect program / erase operation.

The electrical analysis showed also that some of the failing bits are gate stress sensitive. In fact, programming any of the bits of the failing row causes the threshold of the failing bit to increase more and more up to a saturation level. What's more, performing a gate stress on the whole array after electrical erase resulted in a zero current measured only on the failing cell.

We performed also gate stress and drain stress on programmed array resulting in no variation of the charge content.

A failure analysis performed on the dice failing for gate stress after electrical erase shows a remaining strip of poly between the

sensitive bit and the next one. This leads us to suppose that this failure mode can be included in the classification of "resistive shorts between cells".

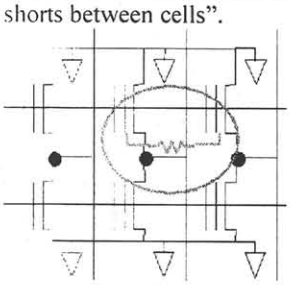

Fig.1: schematic representation of a resistive short between 2 cells

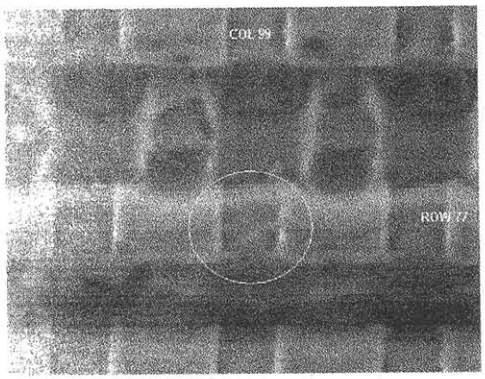

Fig. 2: Poly resistive short between 2 cells

Another interesting finding is the fact that a gate stress performed on UV erased array does not detect all the rejects. The reasons for this are:

1) a lower threshold delta after the stress: in fact the UV threshold distribution is higher than the electrically erased one and then the stress effect is lower;

2) a higher gate voltage used to read the "ones" of the array, being the distribution higher and wider and so determining a less accurate screening. The reference used then is not good enough to detect the cells moving after the stress as showed in the Fig.3.

As we can see from the graph, applying Vgs=7.0v, the current of the failing bit is higher than the reference one. The comparison of the 2 currents makes the failing bit to be still read as a 1.

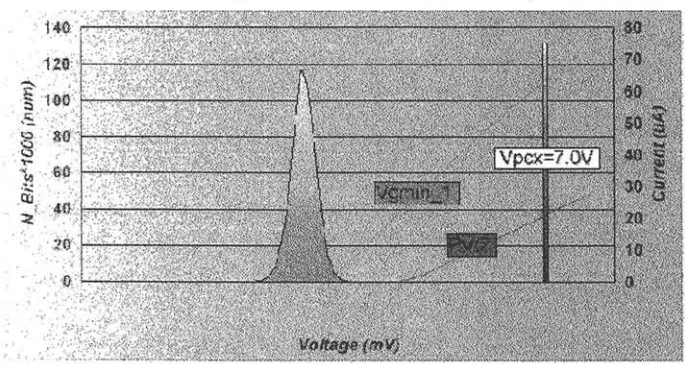

Fig.3: Distribution of thresholds of an erased array

The implication is that we need to perform the screening gate stress after Electrical Erase and not on virgin cells.

Anyway we did not detect only the cells Gate Stress Sensitive (GSS) but also cells sharing charge with the neighbors. We then concluded to implement the screening split in two steps, in order to verify that the gate stress is screening all the bits having stand alone oxide defectivity (GSS) and all resistive shorts or other kind of interaction between cells (RS) could be detected by the CK programming next. The steps are described below:

1) - Electrical Erase;
   - Vgmin;
   - Gate Stress;

2) - Read All1 @ Vgmin + 200 mV;
   - Program CK;
   - CKN Read All1 @ Vgmin + 200 mV;

We tried this new test version on other 40000 dice. We already saw that the GSS failing bits changed their current to zero when a gate stress was performed on erased array, while no change occurred performing a gate stress on programmed failing bits. Again, no difference was detected in the gain of these cells.

RS failing bits, instead, have a current greater than the good one after electrical erase. Programming some of the bits close to the failing ones changes their threshold, but they confirm not to be gate or drain stress sensitive. This can be explained supposing resistive shorts between the failing cells and some of their neighbors.

30000 devices from 3 different lots have been tested in order to verify these trials so far. A bake of 24 hours at 125C previously detecting cells with retention defectivity resulted in 0 pieces failing.

4. CONCLUSION

The trials performed so far were aimed to detect the rejects previously screened using bake and subsequently a screening test in a simpler and cheaper way for production, without causing any reduction of the testing coverage. The analysis performed makes us suppose that the rejects due to charge sharing and retention defectivity can be detected with a gate stress performed after electrical stress and a check of the threshold variations after programming of a part of the array. The gate stress itself is not detecting all the defective cells unless related to the threshold distributions before and after it. The screening performed after a bake on 3 trial lots showed that no further rejects of this kind were detected, resulting in full test coverage of the new approach.

5. ACKNOWLEDGES

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