Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 464-465

C-7-1 (Invited)

Partially-Depleted SOI CMOS for Low-Power-Consumption LSIs

Hiroaki Mikoshiba and Michiru Hogyoku

IC R&D Department, Seiko Epson Corporation
281 Fujimi, Fujimi-machi, Suwa-gun, Nagano-ken 399-0293, Japan
Phone:+81-0266-61-1235 Fax:+81-0266-61-1662 e-mail: mikoshiba.hiroaki@exc.epson.co.jp

1. Introduction

Effectiveness of partially-depleted(PD) SOI technology in a low-power application has been demonstrated by fabricating a SOI watch-IC operating at 0.5V and 30nA [1]. 0.6μm PD device used exhibits strong history effect[2,3]. Although this effect is not a problem in watch-IC, it has been an impediment to the adaptation of PD SOI into mainstream LSIs. MEDICI simulation demonstrates that the history effect can be minimized in scaled down devices at low supply-voltages free from impact-ionization. It is also shown that PD SOI performances are competitive to fully-depleted(PD) SOI in low supply-voltage applications.

2. Watch-IC

PD SOI was employed, because of fabrication easiness, scaling down capability and wide range of applications. Dual-gate and single-drain MOSFETs were fabricated on UNIBOND wafers with Si-layer/BOX thicknesses of 135nm /400nm. Gate oxide thickness is 7nm. Threshold voltage is set at 0.5V in body-tied configuration to obtain off-current of 1pA/μm in floating-body condition. Low threshold-voltage of 0.3V is also used in a key circuit for 0.5V operation.

Fig.1 shows measurement results of transient I_D-V_G characteristics for out-high(V_G=0V/V_D=1V) and out-low(V_G=1V/V_D=0V) initial conditions, compared with body-tied device[3]. Subthreshold slopes are 64 and 80 mV/dec for transient and body-tied, respectively. It is noted that threshold-voltages in floating-body switching operations are 0.05-0.1V lower than those for body-tied device. Large discrepancy between out-high and out-low curves causes history effect.

Fig.2 shows supply voltages vs. circuit currents of fabricated watch-IC, compared to bulk CMOS. Ultra-low power operation of 0.5V/30nA is attained by PD SOI CMOS, while the best performance of bulk CMOS is 0.9V/90nA. Fig.3 shows correlation between threshold-voltages and minimum supply-voltages. SOI can reduce supply-voltage by 0.3-0.4V. This voltage improvement results from floating-body operation(~0.1V), half parasitic capacitance as much as bulk(~0.1V) and low voltage circuit design(~0.1-0.2V). Logic-circuit current is reduced to 1/4.

Analog circuits are biased at subthreshold current range. Voltage-regulation circuit is shown in Fig.4, where bias currents are 2-6nA. Low parasitic capacitance in SOI enables low bias currents. Since output voltage(Vref) is proportional to the sum of threshold-voltages of NMOS and PMOS, and is also proportional to minimum supply-voltage, stable low-voltage operation is guaranteed in wide temperature range.

3. 0.18μm PD SOI

History effect in no impact-ionization region is caused by imbalance between gate- and drain-depletion charges. As gate-length is shrunken, it becomes comparable to Si-layer thickness and charges are balanced. 0.18 μm PD SOI devices were evaluated by using MEDICI. Fig.5 shows the number of holes in out-high and out-low bias conditions. Charge balance in the body region appears at Si-layer thickness of 80nm, where I_D-V_G curves of out-high and out-low overlap and are very close to switching-steady-state characteristics, as shown in Fig.6.

Drain-current in switching-steady-state is 24% larger than body-tied condition of the same device. It is still 7% larger than a body-tied device with reduced body-doping in order to equate off-current to the floating-body device. This results and watch-IC demonstrate positive body-to-source voltage which provides performance gain on floating-body PD devices, even at low drain-voltages.

Fig. 7 compares PD with FD in equal off-current condition. FD has 16% larger on-current for high threshold-voltage device with off-current of $3x10^{-11}$A/μm, because of steeper subthreshold swing. For low threshold-voltage device of $3x10^{-9}$A/μm off-current, however, drain-current gain on FD disappears, as shown in Fig.8. This is because Si-layer thickness of 30nm is not thin enough to prevent punch-through which causes off-current increase.

Fig.9 shows pass-gate-leakage comparison between PD and FD[4]. FD has larger peak value, but total charge of leakage is one order of magnitude larger in PD. Since leakage level is very low, pass-gate-leakage may be insignificant in low voltage applications.

4. Conclusion

5V/30nA watch-IC is brought about by parasitic capacitance decrease, floating body operation of PD SOI and low voltage circuit design. History effect can be minimized in scaled down devices operated at low voltages. Because of difficulty of obtaining perfect FD, PD is attractive even in low voltage applications.

Acknowledgments The authors would like to thank Mr. Ebina and Mr. Kadowaki for their valuable discussions on Watch-IC.

References

[1]H.Mikoshiba et al, 57th Symp. on Semiconductors and Integrated Circuits Technology, Dec. 1999(1999) p.55.
A. Ebina et al, CICC2000,(2000)p.57.
[2]G. Shahidi et al, ISSCC1999, (1999)p.426.
[3]A. Wei et al, IEEE ED, **45**, 430(1998)
[4]F. Assaderaghi et al, IEEE EDL, **18**, 241(1997)

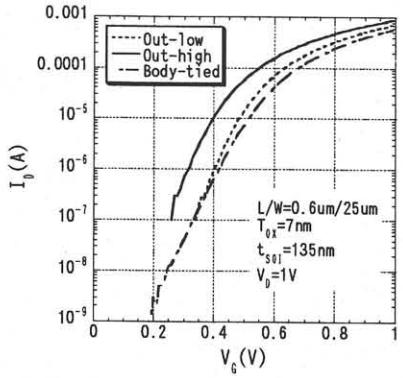


Fig.1 Measurement results of transient characteristics in floating-body operation. Subthreshold slopes are 64 and 80 mV/dec for floating body and body-tied, respectively.

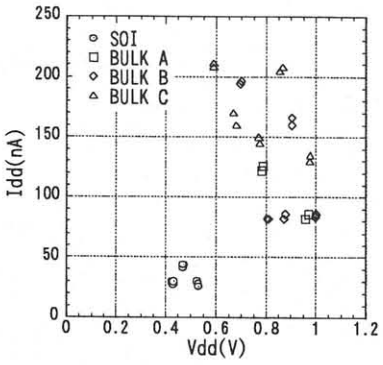


Fig.2 Relationship between supply-voltage and circuit current of watch-ICs.

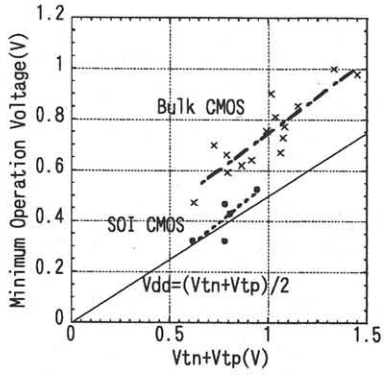
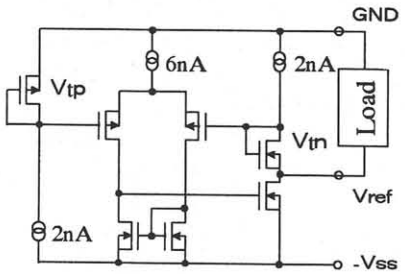


Fig.3 Correlation between threshold voltages and minimum supply-voltages.

Fig.4 Voltage-regulation circuit. Bias current is set in subthreshold region. Output voltage is given by Vref=Vtp + Vtn .



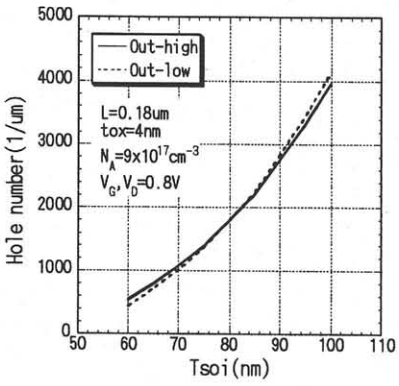


Fig.5 The number of holes in body region of 0.18μm PD NMOS under out-high and out-low conditions as a function of Si-layer thickness. Charge balance is obtained at 80nm.

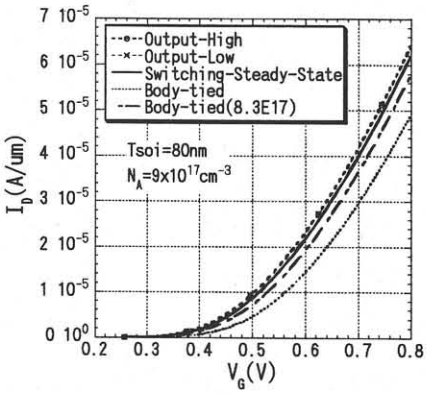


Fig.6 I_D-V_G characteristics of 0.18μm PD NMOS with Si-layer thickness of 80nm, where output-high and output-low characteristics are overlapped.

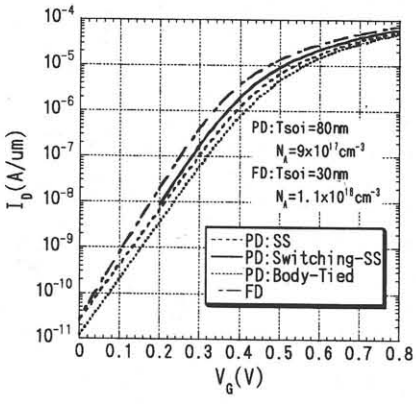


Fig.7 Comparison of drain current between PD and FD at off-current of 3x10^{-11}A/μm. FD is superior to PD in low off-current(high threshold-voltage) device.

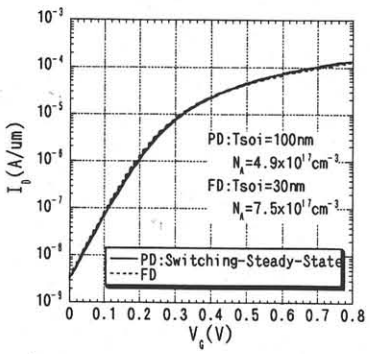


Fig.8 Comparison of drain current between PD and FD at off-current of 3x10^{-9}A/μm. Drain currents are comparable in PD and FD in low threshold-voltage device.

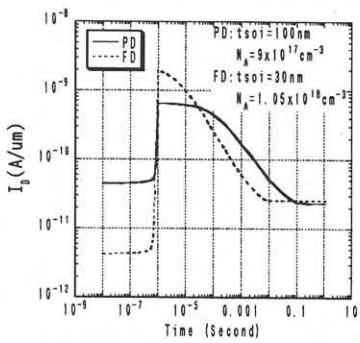


Fig.9 Pass-gate leakages in PD and FD. Peak value is larger in FD, but total leakage charge is larger in PD.