Extended Abstracts of the 2000 International Conference on Solid State Devices and Materials, Sendai, 2000, pp. 468-469

C-7-3

Advanced CMOS Technology on Sapphire Substrate for RF Systems on a Chip

Y.-C. Tseng, *J. Cable, *M. Stuber, *R. Reedy, and J. C. S. Woo

Department of Electrical Engineering, University of California, Los Angeles, CA 90095, USA
*Peregrine Semiconductor Corporation, San Diego, CA 92121, USA

Abstract — CMOS/SOI on a sapphire substrate has shown to significantly improve RF device characteristics. Reduced floating body effects; achievement of high Q on chip components; excellent isolation; and high performance RF circuits enable high performance RF systems on SOS substrates.

Introduction

Rapid growth and increasing complexity of the portable communication applications are forcing miniaturization of the whole system and reduction in total power consumption. Increasing levels of integration up to full systems on a single chip (SOC) is clearly necessary. However, competition between different technologies, especially for RF systems, is based on both passive and active device performance, plus each technology inherent manufacturability. While Bulk CMOS technology has dominated VLSI electronics (especially digital), high flicker noise and multiple substrate effects are still major concerns for RF integration. In this study, the impact of a sapphire substrate on active and passive devices and the resulting RF circuit performance are addressed.

Substrate Technology on Device Performance

CMOS/SOI technology reduces parasitic capacitances; but also creates floating body effects and increases 1/f noise. Transistor f_τ, f_{max} and speed-power product improve, but SIMOX and BESOI substrate materials have large floating body effects and high RF losses. With lossless sapphire (Al_2O_3) substrate, 0.5μm SOS CMOS, fabricated by UTSi (Ultra Thin Silicon on Sapphire) technology [1], can provide 40 and 60GHz f_{max} for 1 and 3V respectively (Fig. 1).

In addition, the short (~5 nsec) minority carrier lifetime suppresses floating body effects, resulting in both a smaller current kink magnitude and a higher kink onset voltage (Fig. 2). This also permits use of fully depleted (FD) devices. However, Si/insulator states can potentially affect the low-frequency (LF) noise performance [2]. Extra trap-assist leakage current (I_G and I_R in (2)) also significantly increases the pre-kink excess noise (Fig. 3). We have reported that excess GR noise has been suppressed and a pure $1/f$ noise is achieved in a wide V_{GT} range in the UTSi technology by reducing the amorphization temperature to below 0°C [2]. Achievement of comparable 1/f noise to bulk CMOS technology, and elimination of bulk-trap related GR noise indicates that the quality of both the gate oxide and silicon film on SOS are close to that of bulk silicon [2].

Inherent Suppression of AC Floating Body Effects

CMOS on SOI is a candidate for RF systems on a chip [3]. However, floating body effects reduce analog gain, degrade linearity and induces LF noise overshoot [4]. At RF, the AC output conductance kink is suppressed by high-pass filtering of S/B junction [4]. However, phase noise overshoot still exists due to the upconversion of the excess LF noise [5]. Both AC kink and LF noise overshoot result from body instability due to frequency dependence of the S/B junction impedance as follows,

$$Z_{Body} = \frac{r_{SB}}{1 + j\omega \cdot r_{SB} C_{BB}} \text{ and } r_{SB} = \frac{nV_T}{I_{SB} + I_R} \quad (1)$$

where $I_{SB} = I_R \cdot (e^{V_{SB}/nV_T} - 1)$ is the S/B junction current and is dominated by impact ionization current (I_{ii}) at larger drain bias. In the SOS technology, I_R is large (due to the recombination center at the silicon/sapphire interface) which suppresses AC kink and LF noise overshoot in low frequencies (Fig. 2 & 4). As a result, back interface in SOS technology is an advantageous factor for implementing RF IC's in SOI CMOS technology.

Integration Issues

Having both PD and FD transistors on a single chip is an attractive option for RFIC SOC design. Implementation in UTSi CMOS is accomplished with a single implant step. PD transistors (with body ties to eliminate floating body effects when necessary) can be used in logic and I/O blocks while FD devices (with lower V_{TH} and higher g_m/I_D) for RF analog blocks. In addition, unlike FD SOI/SIMOX device [4], FD SOS shows a drain-bias independent $1/f$ noise from threshold to strong inversion (Fig. 5), suggesting that it can be used for noise sensitive RF blocks.

A. On-chip components and Isolation

Inductors are the most challenging passive component in lossy silicon substrate. Q (quality factor) greater than 10 and f_{sr} (self-resonant frequency) 3X higher than the operating frequency are desired [6]. With the lossless sapphire substrate and only 3 Al metal layers, a 4nH inductor with Q_{max} above 15 and f_{sr} above 13GHz (Fig. 6) is easily achieved. Isolation is another strict requirement for mixed mode/RF applications. It is doubtful that a finite thickness of buried oxide can efficiently block the penetration of RF signals. Fig. 7 shows that the inductor coupling in UTSi technology with 30dB isolation between two large planar inductors. More importantly, it shows 5dB and 10dB improvement of pad isolation @ 2GHz over SIMOX and bulk silicon substrates, respectively. Therefore, the completely insulting SOS technology yields excellent RF signal isolation.

B. Critical RF Circuit Performances

Excellent IIP_3 in SOS mixer has been reported [6]. Performance of RF switch, PLLs, VCOs, EEPROM, and power amplifiers (PA) are also critical for integrating RF functions in CMOS. Currently, GaAs or BJT technologies dominate these building blocks. Fig. 9 shows the measured performance of RF switches on SOS at 2GHz. 0.5dB insertion loss and up to 20dBm power handling capability are achieved. Such excellent RF switch performance, comparable to the best GaAs switch, is a direct result of an insulating substrate. Fig 10. shows a low power, low phase noise phase locked loop (PLL) on UTSi SOS substrate. Addition of a high-Q tank circuit and proper oscillator design will enable fully integrated VCOs. In addition, a zero mask EEPROM/Flash cell was reported [7].

Power amplifier is a challenge for SOI CMOS. Even with optimized body contact and drain engineering, the large thermal resistance of the buried oxide still limits large power operation of most SOI technology. This, however, is not a problem for SOS due to its 2x thermal conductivity over silicon. In addition, unlike GaAs, SOS is not brittle, making wafer thinning easier. A 25dBm PA with > 50% PAE has been simulated (Fig. 11).

Conclusion

In this study, the impact of sapphire substrate on device performance has been discussed in detail. Inherently weaker

floating body effect of SOS device alleviates the complexity of transferring bulk silicon CMOS to SOI CMOS technology. The issues for integrating RF systems on a chip are also addressed. Low loss sapphire substrate can further extend leverage of SOI circuits towards much higher operating frequency. In addition, suppressed AC floating body effects and good thermal conductivity in sapphire substrate can enable the integration of complex RF SOC.

References

[1]R. Reedy, et al., *SOI Conf.*, p.8, 1999.
[2]Y.-C. Tseng, et al., *SSDM*, p.368, 1999.
[3]W. M. Huang, et al., *CICC*, p.421, 1997.
[4]Y.-C. Tseng, et al., *VLSI Tech.*, p.112, 1998.
[5]Y.-C. Tseng, et al., *EDL*, p.54, 1999.
[6]M. Stuber, et al., *SOI Conf.*, p.70, 1997.
[7]R. Reedy, et. al. GOMAC, March 2000.
[9]J. Raskin, et al., *TED*, p.2252, 1997.

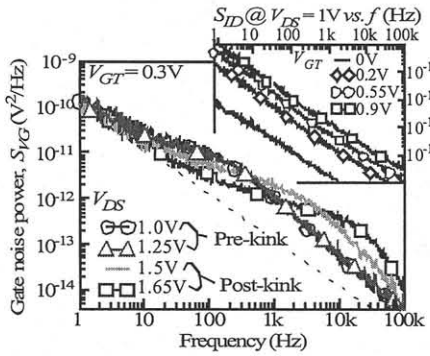

Fig. 3: LF noise characteristics of a PD SOS nMOS with original process. Inset shows the pure $1/f$ noise in a wide V_{GT} range for advanced process. Excess noise can be expressed as [7],

$$S_{VG,\,excess} = \frac{4q(nV_T)^2}{1+(f/f_0)^2} \cdot \frac{I_G+I_{ii}}{(I_G+I_{ii}+I_R)^2} \cdot \beta^2 \quad (2)$$

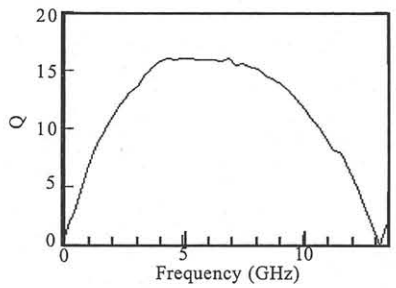

Fig. 6: Measured Q of a 4nH inductor versus frequency.

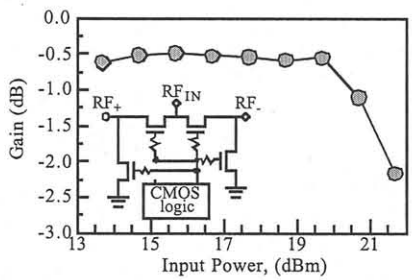

Fig. 9: Insertion loss of a RF switch measured at 2GHz built on sapphire substrate. Inset shows the schematic circuit diagram.

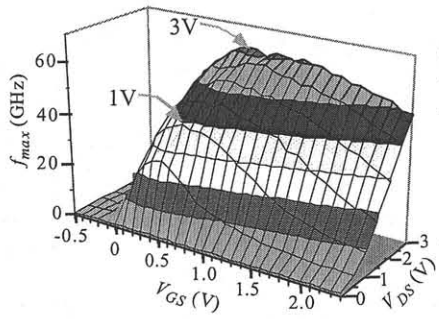

Fig. 1: f_{max} of FD floating body SOS nMOS with W/L = 250/0.5μm (L_{eff} = 0.35 μm) as a function of gate and drain biases.

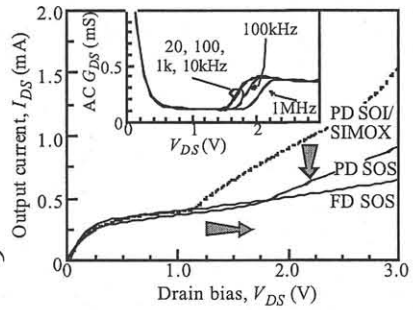

Fig. 2: Output characteristics of PD, FD SOS and PD SOI/SIMOX nMOS (L_{eff} = 0.65μm) biased at 0.3V V_{GT}. Inset shows AC G_{DS} of PD SOS nMOS.

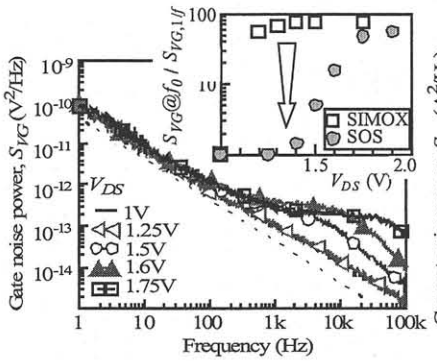

Fig. 4: LF noise overshoot of a PD SOS nMOS (L_{eff} = 0.65μm) biased at V_{GT} = 0.3V. Inset shows the relative noise overshoot magnitude in SOS compared with that of SOI/SIMOX.

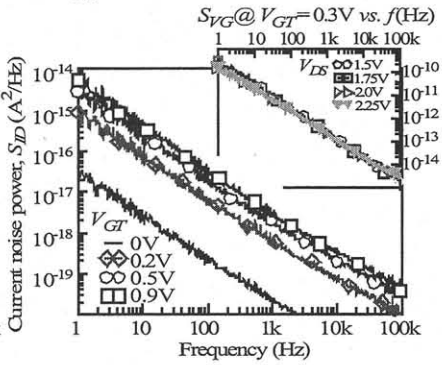

Fig. 5: Output current noise characteristics of a FD SOS nMOS (L_{eff} = 0.65μm) biased at V_{DS} = 1V. Inset shows the drain-bias independent gate noise power.

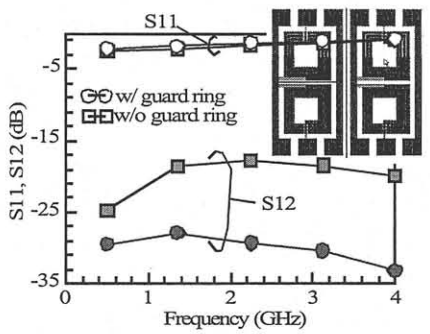

Fig. 7: Isolation between two large planar inductors at very close spacing, with minimal capacitive guard ring. Inset shows the test layout.

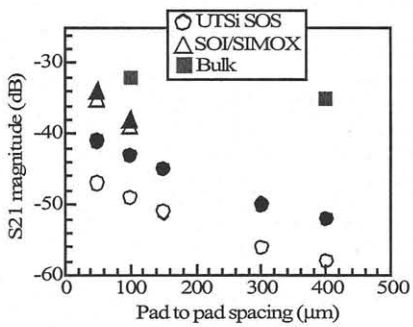

Fig. 8: Comparison of pad to pad isolation of different substrates as a function of pad distance, measured at 1GHz (opaque symbols) and 2GHz (filled symbols). Bulk and SIMOX data from [8], [9].

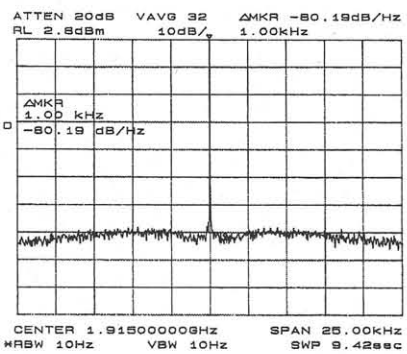

Fig. 10: Integrated 2GHz Phase locked loop (PE3236) performance measured at 100kHz channel spacing built on SOS technology.

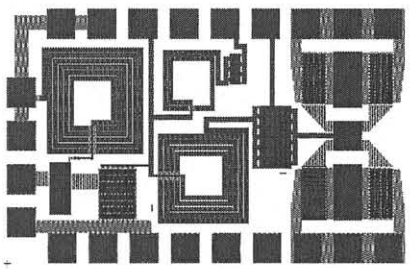

Fig. 11: 2 stage Class-C power amplifier on SOS with 50Ω output matching. Simulated results show 25dBm P_{out}, 19dB Gain and 53% PAE while operating at 850MHz and 2.5V power supply. It is under fabrication now.