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On the Temperature Dependence of Hysteresis Effect in Floating-Body Partially-Depleted SOI CMOS Circuits

R. Puri, C. T. Chuang, M. B. Ketchen, *M. M. Pelella, and M. G. Rosenfield
IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, U. S. A.(puri@watson.ibm.com)
*University of Florida, Gainesville, FL 32611, U. S. A.

1. Introduction

As the scaling of CMOS approaches the end of the roadmap, lowering the operating temperature of CMOS circuits improves the device and circuit performance due to higher transistor current resuling from higher mobility, steeper subthreshold slope [1,2]. The temperature dependence of partially-depleted (PD) SOI CMOS devices and circuits is significantly more complicated than the bulk CMOS. The physical mechanisms determining the body potential for various initial DC equilibrium conditions and steady-state are fundamentally different [3,5], resluting in distinctly different temperature dependence. This paper presents a detailed study on the temperature dependence of hysteresis effect in static CMOS inverter, single-ended LEAP circuit,and cross-coupled dual-rail CPL circuit in a 1.5 V, $L_{eff} = 0.08\ \mu m$ PD/SOI technology with $t_{OX} = 2.3$ nm, $t_{Si} = 150$ nm, and $t_{BOX} = 145$ nm.

2. Static CMOS Inverter

Fig.1(a) shows the input-rise delays as functions of time for a PD/SOI CMOS inverter with temperature as a parameter. The inverter input is initially at "Low" and then continuously switches at 1.0 GHz with 50% duty cycle and 100ps input slew. The corresponding body voltages for the nMOS are shown in Fig.1(b). With the initial input at "Low", the initial body potential of the nMOS sits at a diode cut-in voltage determined by the balance of the reverse-biased drain-to-body diode leakage and forward-biased body-to-source diode current [3]. Hence the initial nMOS body voltage and the initial input-rise delay exhibit strong temperature dependence. Moreover, as the temperature is lowered, both the initial body potential and the steady-state body potential increase, thus further improving the input-rise delays. Consequently, the PD/SOI inverter has more significant performance improvement compared with the bulk CMOS. Fig.2(a) and 2(b) show the complementary situation, where the inverter input is initially at "High". With both the drain and source at "GND", the initial body voltage of the nMOS is at "GND". As the gate signal rampes down and the drain voltage goes up, the body voltage is capacitively coupled up by the drain-to-body capacitance [3]. Hence, the body voltage of the nMOS before the first input-rising transition is determined primarily by capacitive coupling and exhibits weak temperature dependence (evident by the "clustering" of the initial body voltage in Fig.2(b)). The initial input-rise delay thus exhibits a very weak temperature dependence (Fig.2(a)). Fig.3 shows the first "input-rise" delays for the two initial states as functions of the temperature. The case with the initial state at "Low" can be seen to exhibit significantly higher temperature dependence than the case with initial state at "High", and the cross-over for the two cases (at around 55 °C) can be clearly seen. Also shown are the complementary situations (dictated by the pMOS) for the first "input-fall" delays for the two initial states with the cross-over around 0 °C. The steady-state is independent of the initial states of the circuit, since it is determined only by the net charges gained/lost through the switching cycle and is reached when the net charges gained/lost through the switching cycle equal to zero. Fig.4 depicts the net charges injected/removed by each body charging/discharging mechanism during the first switching cycle as functions of the temperature. The body charges injected by the reverse-biased drain-to-body diode and the body charges removed by the forward-biased body-to-source junction decrease with lowered temperature with a strong temperature dependence. The body charges injected by the impact ionization current increase with lowered temperature with a mild temperature dependence [4]. The "net" charges (sum of the three mechanisms) increase with lowered temperature with a weak temperature dependence. Thus, the steady-state delay decreases with lowered temperature with a weak temperature dependence (Fig.5). Furthermore, a slower input slew (200ps in Fig.5) increases the cross-over region during the switching transient and the impact ionization current component in the "net" charges, resulting in a stronger temperature dependence (compared with the 100ps input slew case).

3. Single-Ended LEAP Circuit

If a LEAP circuit [5] (Fig.6) is initially conditioned to a state with both "IN1" and "OUT" at "High", the body voltage of the front-end nMOS pass-transistor will be at V_{DD} to start with. If it is initially conditioned to a state with both "IN1" and "OUT" at "Low", the body-voltage of the front-end nMOS pass-transistor will be at GND to start with. For both cases, when the select input A switches to "High", the body voltage of nMOS qA is capacitively coupled up by the large gate-to-body capacitance. Thus, the initial body voltage of the nMOS pass-transistor is determined by capacitive coupling and exhibits a very weak tenperature dependence in both cases. For the back-end inverter, with the initial input conditioned to the "High" state, the initial body voltage of the nMOS before the "input-rising" transition is determined by the capacitive coupling, thus exhibiting a very weak temperature dependence. Moreover, the increased V_T at lowered temperature and the V_T loss in passing a "High" state through the nMOS pass-transistor offset the enhanced mobility and improved current drive, resulting in a relatively weak negative temperature dependence as shown in Fig.6(a). For the back-end inverter, with the initial input conditioned to the "Low" state, the initial body-voltage of the nMOS is determined by back-to-back diode, resulting in a stronger temperature dependence in the first "input-rise" delay than the case with the initial state at "High" (Fig.6(a)). For the "input-fall" delay, the increased V_T at lowered temperature and V_T loss through the pass-transistor lowers the "High" level at the input of the inverter and bring it closer to the threshold of the inverter, thus further improving the "input-fall" delay and resulting in very significant temperature dependence (Fig.6(a)). The same effect, that the "input-fall" delay decreases significantly and exhibit much stronger temperature dependence than the "input-rise" delay, can also be observed for the steady-state "input-rise" delay and "input-fall" delay (Fig.6(b)).

4. Dual-Ended CPL Circuit

For cross-coupled dual-rail CPL circuit (Fig.7) the "rising input" delay and its variation and temperature dependence are compensated by the "falling input" of the other branch, and vice versa [5]. Because of this compensation effect, the "input-rise" delay for this dual-ended CPL circuit exhibits stronger temperature dependence (and decrease at lowered temperature) than single-ended LEAP circuit (Fig.7(a), 7(b)). Corresponding compensation effect on "input-fall" delay is also evident.

5. Conclusion

We have presented a detailed study on the temperature dependence of hysteresis delay variations in PD/SOI CMOS circuits. It is shown that depending on the initial state of the circuit, the initial circuit delays have distinct temperature dependence. For steady-state circuit delays, the temperature dependence is dictated solely by the various charge injection/removing mechanisms into/from the body. Use of cross-coupled dual-rail configuration in pass-transistor circuits was shown to be effective in compensating and reducing the disparity in the temperature dependence of "input-rise" delay and "input-fall" delay.

References

[1] F. H. Gaensslen et al., "Very small MOSFETs for low temperature operation," IEEE Trans. Electron Devices, vol. ED-24, 1977, p.218.
[2] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, New York, 1998.
[3] M. M. Pelella et al., "Hysteresis in Floating-Body PD/SOI Circuits," Intl Symp. on VLSI Tech.,Syst.,Applications, Taiwan, 1999, p.278-281.
[4] S. M. Sze, Physics of Semiconductor Devices, 2nd edition, John Wiley and Sons, New York, 1981.
[5] R. Puri and C. T. Chuang, "Hysteresis Effect in Pass-Transistor Based Partially-Depleted SOI Circuits," IEEE Intl SOI Conf., 1998, p.103-104.

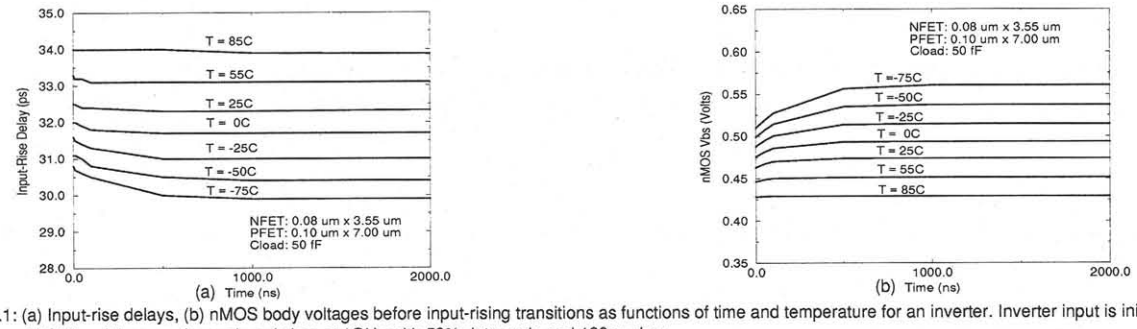


Fig.1: (a) Input-rise delays, (b) nMOS body voltages before input-rising transitions as functions of time and temperature for an inverter. Inverter input is initially at LOW and then continuously switches at 1GHz with 50% duty cycle and 100ps slew.

Fig.2: (a) Input-rise delays, (b) nMOS body voltages before input-rising transitions as functions of time and temperature for an inverter. Inverter input is initially at HIGH and then continuously switches at 1GHz with 50% duty cycle and 100ps slew.

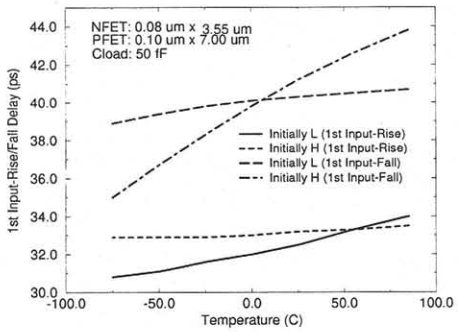


Fig.3: First 'input-rise' delays and first 'input-fall' delays for an inverter as a function of temperature for two initial conditions (inverter input initially a LOW or at HIGH)

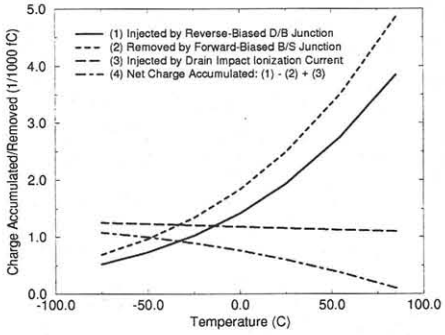


Fig.4: Charges injected/removed into/from body of nMOS by various mechanisms in the first switching cycle as function of temperature (inverter input initially LOW)

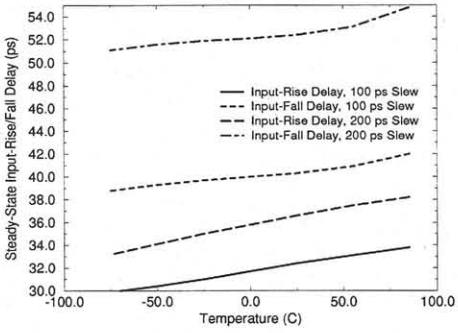
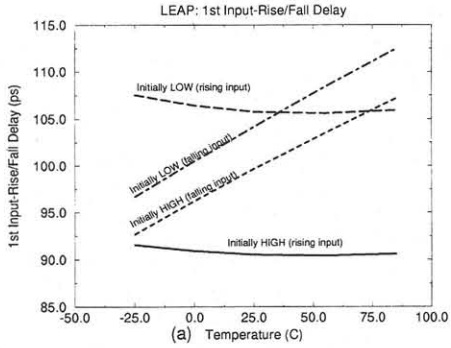
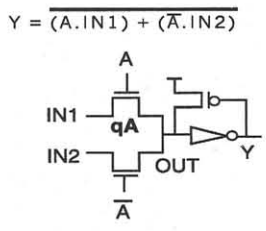


Fig.5: Steady-state 'input-rise' delay and 'input-fall' delay for 100ps and 200ps input slew as function of temperature for an inverter.





Schematic of a single-ended LEAP circuit

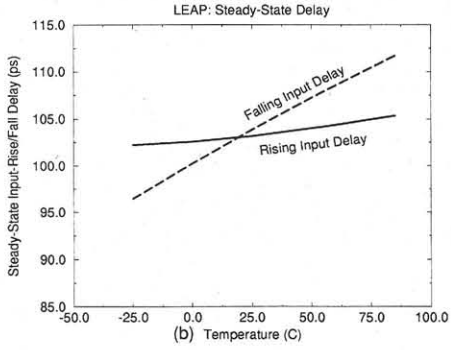
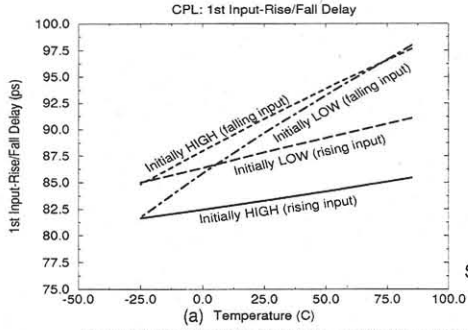
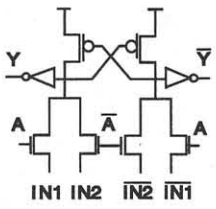


Fig.6: (a) First 'input-rise' delays and first 'input-fall' delays (b) steady-state 'input-rise' delay and 'input-fall' delay as functions of temperature for LEAP circuit.





Schematic of a cross-coupled dual-rail CPL circuit

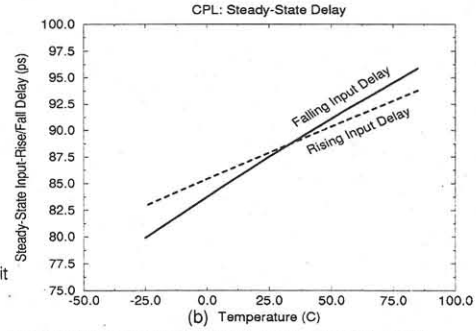


Fig.7: (a) First 'input-rise' delays and first 'input-fall' delays (b) steady-state 'input-rise' delay and 'input-fall' delay as functions of temperature for CPL circuit.