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A Novel Fabrication Technique of Ultra-Thin and Relaxed SiGe Buffer Layers with High Ge Content for Sub-100 nm Strained Silicon-on-Insulator MOSFETs

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1. Introduction

As a promising device structure to realize low power consumption and high-speed CMOS circuits, we have already demonstrated p- and n-type strained Si-on-insulator (SOI) MOSFETs with the gate length L_g down to 0.25 μm [1, 2]. This structure requires relaxed $Si_{1-x}Ge_x$ buffer layers on buried oxide (BOX) layers (SiGe on insulator; SGOI), on which strained-Si films are grown. Although we have successfully fabricated 300 nm thick SGOI layers with the Ge content x=0.1, much thinner relaxed SGOI (<20 nm) layers with x>0.3 [3] are strongly required in order to realize fully-depleted strained SOI MOSFETs with L_g < 100 nm and large mobility enhancement. However, such the SGOI structure is quite difficult to be fabricated by SIMOX technology [4]. Another method, reported so far, is composed of the epitaxial growth and post-annealing of a SiGe layer on a thin SOI [5]. However, this method is not suitable either for the fabrication of the short channel MOSFETs because of introduction of high density of dislocations in the SOI layer. In this paper, we demonstrate a novel fabrication technique to obtain relaxed and ultra-thin SGOI structures with high Ge content and low dislocation density. This technique is based on the rejection of Ge atoms from SiGe oxide layers and the condensation in the SGOI layer. We have successfully fabricated a relaxed 16 nm-thick SGOI with x=0.57, which is applicable to sub-100 nm SOI MOSFETs with strained-Si or SiGe channels.

2. Fabrication procedure of SGOI structures

The fabrication procedure of SGOI structures is outlined in Fig. 1. (a) At first, graded SiGe and uniform $Si_{0.9}Ge_{0.1}$ layers are grown on (001) Si substrates by ultra-high vacuum chemical vapor deposition. (b) Next, BOX layers are formed by the SIMOX technique, which results in 320 nm-thick SGOI with x=0.08±0.01 [1]. In some wafers, the thickness of SGOI is reduced down to 185-100 nm by chemical etching. (c) Finally the wafers are oxidized at 1050 ℃ in dry O_2. One of possible application of the present SGOI layers to MOSFET structures is shown in (d).

3. Results and discussions

Figure 2 shows the Auger electron spectroscopy (AES) depth profiles of Ge in the SGOI layers fabricated in the procedure shown in Fig. 1. The profiles show that the Ge content near the oxide/SiGe interface increases and the Ge atoms are condensed into the SGOI layer, as the oxidation proceeds. It was found by the SIMS measurement that the Ge concentration in the oxide is of the order of $1x10^{18}$ cm^{-3}. The total amount of Ge atoms in the SGOI normalized by the value before oxidation is plotted versus oxidation time in Fig.3. The amount is kept constant during the oxidation. This conservation of Ge atoms and low Ge concentration in the oxide layer mean that the oxidized SiGe layer rejected Ge atoms and left them into the SGOI layer and that the surface oxide layer as well as the BOX layer act as the barrier for the Ge diffusion. The nonuniformity of the Ge content in Fig. 2 was reduced by annealing the SGOI in N_2 gas due to Ge diffusion as shown in Fig. 4. SGOI layers with the thickness below 20 nm and x>0.3 were obtained by oxidizing the SGOI layers with the initial thickness below 160 nm. Cross sectional TEM images of 16 nm-thick SGOI layer are shown in Fig. 5. A clear lattice image indicates that Ge atoms rejected from the oxidized layer finally locate at the lattice points. Only a few threading dislocations were observed in the TEM field of about 20 μm. It is found from the EDS analysis as shown in Fig. 6 that the Ge content, which is quite uniform across the SGOI, amounts to as high as 57 %. Figure 7 shows the peak shifts of the Raman spectra for the SGOI layers with the thickness of 200-16 nm as a function of the averaged Ge concentration. These values coincide well with the theoretical ones for fully relaxed SiGe alloy [6], meaning that the present SGOI layers are fully relaxed. It is concluded that the thinning of the SGOI, the condensation of Ge and the lattice relaxation proceed simultaneously during the oxidation.

4. Conclusion

A novel fabrication technique of ultra-thin SGOI with high Ge concentration was proposed. Using this technique, 16 nm-thick SGOI with x=0.57 was demonstrated. This is a promising technique for the application to sub-100 nm fully-depleted SOI MOSFETs with strained-Si or SiGe channels.

Acknowledgments

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References

[1] T. Mizuno et al., IEDM Tech. Dig. 934 (1999), [2] T. Mizuno et al., IEEE Electron Device Lett., to be published, [3] R. Oberhuber et al., Phys. Rev. **B 58**, 9941 (1998), [4] Y. Ishikawa et al., Appl. Phys. Lett., **75**, 983 (1999), [5] A. R. Powell et al., Appl. Phys. Lett. **64**, 1856 (1994), [6] B. Dietrich et al., J. Appl. Phys. **74**, 3177 (1993)

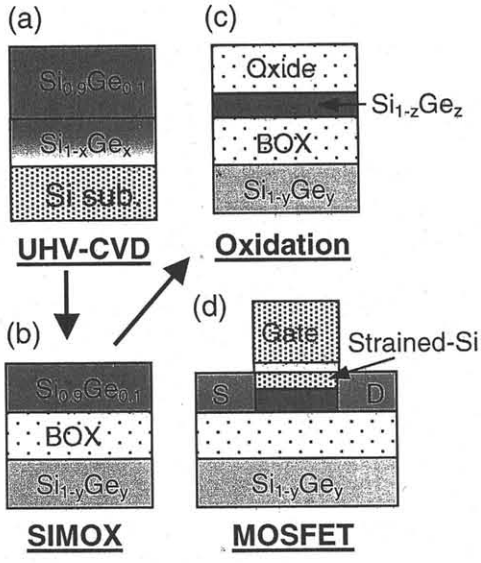

Fig. 1 The Fabrication procedure of the SGOI structure (a-c) and possible application of the SGOI layers to MOSFET structures (d). Here, x varies from 0 to 0.1 toward the surface, y<0.1 and z>0.5.

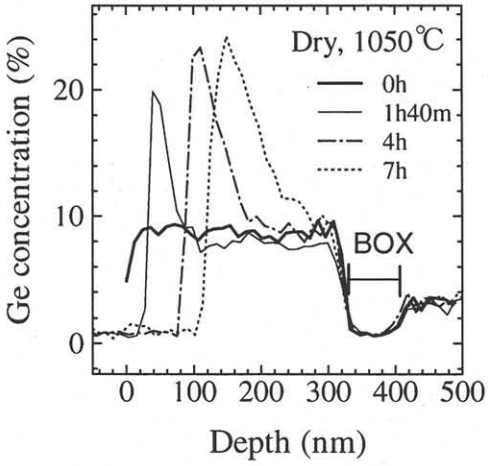

Fig. 2 Depth profiles of Ge in the SGOI layers analyzed by sputtering AES before and after oxidation for 1 h 40 m, 4 h and 7 h.

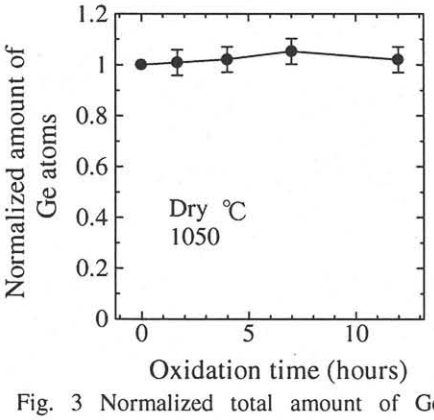

Fig. 3 Normalized total amount of Ge atoms as a function of oxidation time. The total amount was obtained by integrating the depth profile of Ge across the SGOI, and then the integrals were divided by the value before oxidation.

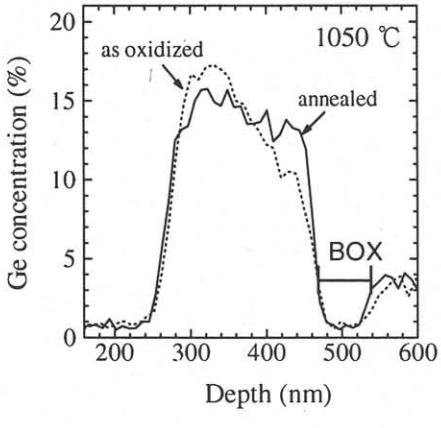

Fig. 4 Depth profiles of Ge in the SGOI layers analyzed by sputtering AES after 12 h oxidation (dotted line) and after 12 h oxidation and 12 h post annealing (solid line).

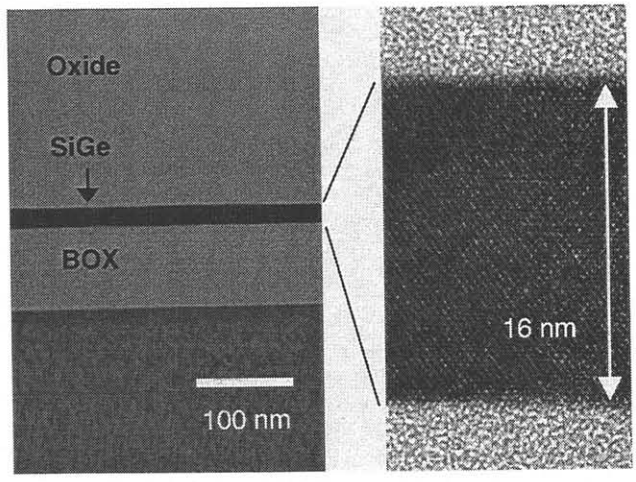

Fig. 5 TEM images of 16 nm-thick SGOI. The clear lattice image indicates a good crystal quality.

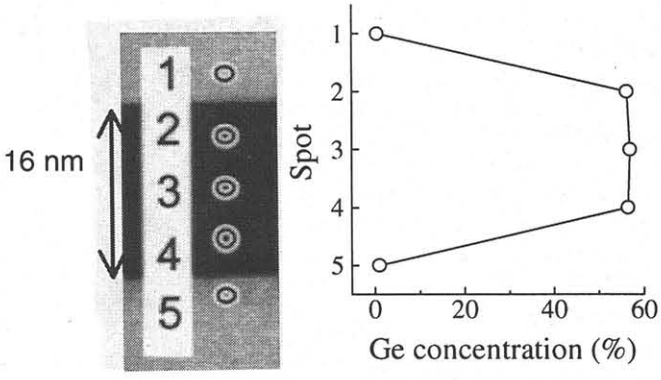

Fig. 6 The depth profile of Ge in the 16 nm-thick SGOI analyzed by EDS. The left image shows the analyzed spots. Electron beam size is about 1 nm in diameter.

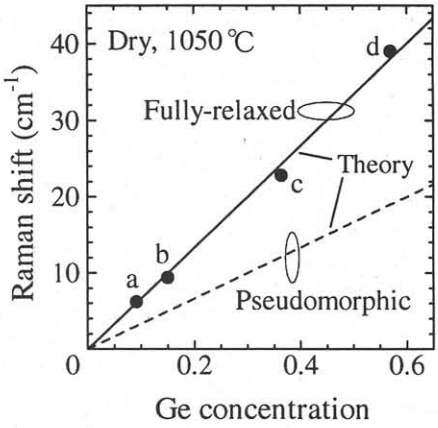

Fig. 7 Peak shifts of Raman spectra from that of Si for the SGOIs with the thickness of (a) 320 nm (as SIMOX), (b) 200 nm, (c) 40 nm, and (d) 16 nm. The observed peaks correspond to the Si-Si mode. Theoretical values for fully relaxed SiGe alloy and pseudomorphic SiGe layer on Si substrate are also shown [6].